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Balanced Comparator and Delta-Sigma Modulator with High-T_c Multilayer RSFQ Logic Circuits

고온초전도 다층박막 RSFQ 회로를 이용한 균형잡힌 비교기와 델타-시그마 모듈레이터

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We demonstrate small-scale high-T_c superconductor RSFQ(Rapid Single Flux Quantum) circuits using multilayer bicrystal technology. An RSFQ balanced comparator is demonstrated with good current resolution, and its operating conditions are discussed in some detail. A single-loop delta-sigma modulator is realized adding a feedback loop to the comparator. The effect of the feedback is confirmed by dc measurement and simulation. A design of an RSFQ toggle flip-flop with the same multilayer bicrystal technology is suggested.

1. Introduction

Rapid single flux quantum(RSFQ) logic has been suggested as competitive candidate for a low power ultra-fast superconducting electronics [1]. Various circuits have been developed with low-T_c superconductors, and several small-scale circuits have been recently demonstrated with high-T_c superconductor.

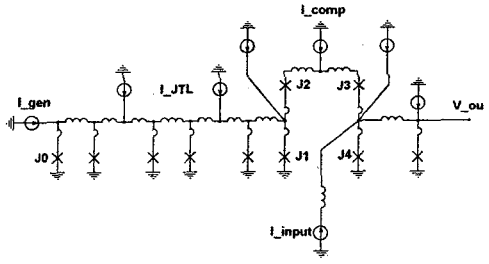
The ground plane is essential for small inductances required for proper RSFQ circuit operation with large critical current junctions. Since high-T_c multilayer Josephson junction technology is still premature, we adopted bicrystal junctions in multilayer thin films to demonstrate high-T_c RSFQ circuits with ground plane[2]. Here we report a successful fabrication and operation of a balanced comparator and delta-sigma modulator.

2. Balanced Comparator

2-1. Fundamentals

The balanced comparator is the basic RSFQ component, which consists of two series -connected Josephson junctions[3]. It compares the input current with some reference value, and gives a single flux quantum(SFQ) voltage pulse output at the clock frequency when the

input is greater than the reference. Since RSFQ logic enables very fast sampling rate up to several hundred GHz, high dynamic response is possible. When the comparator receives a SFQ pulse, one of the two junctions should change its phase by 2π. Exactly which junction to switch is determined by the additional input current into the central node of the comparator. The reference current level can be adjusted by adding a constant offset current to the current input. Depending on whether the current input is higher or lower than the reference level, every incoming sampling pulse will switch either the upper(J3) or the lower(J4) junction, and leave the state of the other junction unchanged. Output SFQ pulses are generated only when the lower junction switches.



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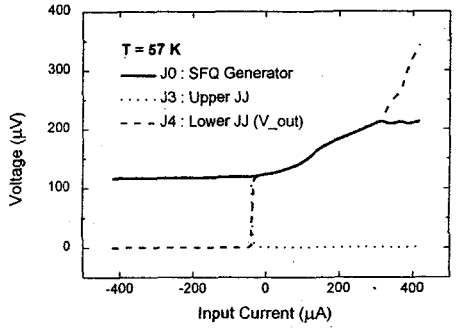


(b)

Figure 1 (a) the circuit diagram of the balanced comparator (b) operation of the balanced comparator at 57K with V_g = 120 μV, or 60 GHz equivalently.

2-2. Design and Operation

Figure 1(a) shows the circuit diagram of the fabricated balanced comparator. It consists of a generator junction(J0), Josephson transmission line(JTL), SFQ buffer(J1,J2) and the comparator (J3,J4). The JTL is biased by a single current source through PdAu on-chip resistors. This is just the part of the delta-sigma modulator explained in the next section.

Operation of the comparator is shown in the figures 1(b). The generator junction was biased at a constant voltage state and generates sampling SFQ pulses with a frequency proportional to the bias voltage. The SFQ pulses are put into the balanced comparator through the JTL and the buffer stage.

As we increase the input current, the output voltage abruptly changes from zero to generator voltage (sampling frequency divided by the Josephson characteristic frequency 483MHz/μV). As we increase the input current further, the output voltage ceases to follow the generator voltage, at which point the comparator cannot sustain the high pulse rate. We measured the comparator operation up to 73 K, however, obviously it would work at higher temperatures than 77 K.

2-3. Current Resolution

As we see in figure, the transition is not perfectly abrupt near input~reference, where each of the junction has a finite probability of switching. The effective transition width (current resolution) ΔI of this gray zone affects essentially on the sensitivity of the SFQ analog-to-digital converters(ADC's), and also reduces the parameter margins. It is known that ΔI depends on several factors such as the speed of the driving pulse train, the effective output impedance of the driver, the energy scale of the thermal and quantum fluctuations, etc. Therefore, it is important to find a proper working point with the smallest ΔI. It is also known that this current resolution is dependent

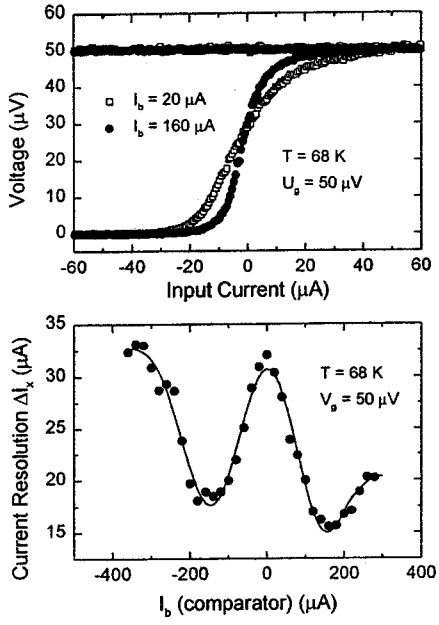


Figure 2 The change of the current resolution according to the bias current I_comp at 68K with V_g = 50 μV.

on the bias current on the comparator loop(I_comp). Figure 2 shows the change in the effective width for different bias current at 68 K with V_g = 50 μV. As we change the bias current, the current resolution changes periodically as shown in the figure. This period of the working point is also dependent on temperature. As temperature increases, the period decreases. This can be understood if we take the total inductance of the comparator loop(J1-J4) into account. Since the kinetic inductance increases steeply in the temperature range of interest, the inductance per square also increases. Hence we need less current in putting a flux quantum into the loop.

3. Delta-Sigma Modulator

3-1. Fundamentals

By adding a feedback loop to the comparator, a single loop superconducting delta-sigma(Δ-Σ) modulator was implemented. The delta-sigma modulation is a technique for increasing the S/N ratio by oversampling and feedback. The basic principle of this technique is that the feedback re-shapes the spectrum of the quantization noise, pushing most of the noise power to high frequencies, well outside the signal band, and then out-of-band signal is removed by the digital filter. While conventional AD/DA converters require high -accuracy analog components in order to achieve high overall resolution, the delta-sigma modulation can trade resolution in time for resolution in amplitude in such a way that imprecise analog circuits may be used.

RSFQ has the unique advantage that very fast sampling rate is possible. This enables large oversampling ratio, which is essential in high-resolution high-speed AD/DA converters. Noise shaping in low-T_c superconducting Δ-Σ modulators has been already demonstrated using niobium technology[4]. High-T_c superconductor results were also presented recently by the same group[5].

The essential difference between the usual PCM(Pulse Code Modulation) and sigma-delta ADCs was described in the excellent review by Candy and Temes[6]. Sigma-delta uses an integrator to continuously sum the sampled analog signal (the Σ operation). This integrated signal is converted to a digital word. A feedback mechanism subtracts this quantity from the total integrated signal (the Δ operation).

Quantization of a signal introduces inevitable quantization error $e < \pm 1/2$ LSB, and this can be treated as noise. The oversampling ratio(OSR), defined as the ratio of the sampling frequency f_s to the Nyquist rate $2f_o$, is given by the number

$$OSR = f_s/2f_o$$

It is well known that simple oversampling reduces the in-band rms quantization noise n by the square root or the oversampling ratio,

that is,

$$n = e/\sqrt{OSR}$$

The signal to noise and distortion(SINAD) is defined as the rms of the fundamental divided by the sum of all spectral components in the passband excluding the dc component. The effective resolution N is then given by

$$SINAD = (6.02N + 1.76)\ dB$$

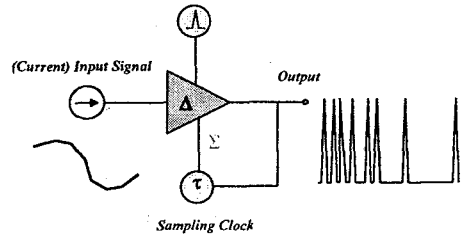
Therefore, each doubling of the sampling frequency decreases the in-band noise by 3 dB, increasing the resolution by only 0.5 bit.

In case of the first-order delta-sigma modulation, the feedback reduces the noise at low frequencies by re-shaping the originally uniform spectral noise density as

$$N(f) \propto (1/\sqrt{f_s})\ \sin(w/2f_s)$$

If the sampling frequency is much higher than the signal band, the noise power that falls into the signal band is,

$$n \propto e/(OSR)^{3/2}$$



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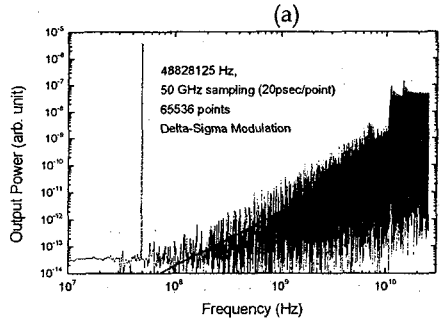
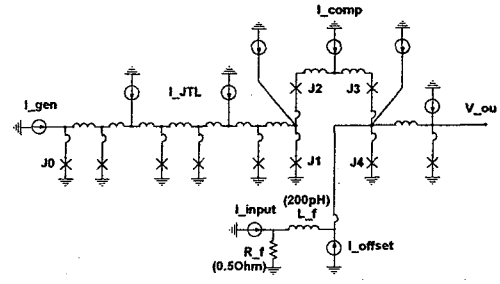


(b)

Figure 3 (a) basic principle of the delta-sigma modulator (b) simulation result of the noise-shaping by the modulation

Therefore, each doubling of the oversampling ratio thus reduces this noise by 9 dB and provides 1.5 bits of extra resolution.

Since the delta-sigma modulator does not require precise component for quantization, this fits itself well into the relatively less mature superconducting technology. Figure 3 shows the basic principle and the simulation result for a single loop delta-sigma modulator. In this simulation, the power spectrum of the PCM-encoded modulator output is obtained by fast Fourier transform(FFT). For calculation, 65536 sampled points were taken, and 50 GHz sampling is assumed, corresponding to 20 picoseconds between each sampled point. A pure sinusoidal signal of 48.8 MHz is used for input(OSR=50). Noise shaping by the feedback



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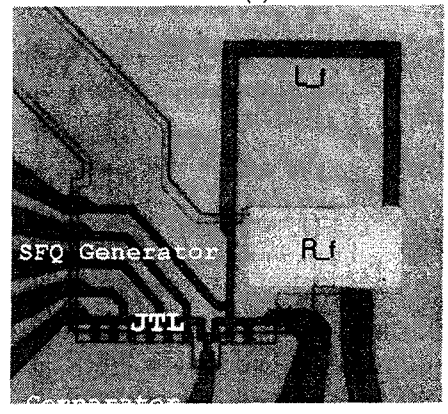


(b)

Figure 4 (a) circuit diagram of the single-loop delta-sigma modulator
(b) photograph of the fabricated circuit

is clearly seen in the figure. The above-calculated noise spectral density is drawn together for comparison.

3-2. Design

Figure 4 shows the circuit diagram of our single-loop delta-sigma modulator and the photograph of the fabricated circuit. The comparator itself is just the same as what we described in the previous chapter. A simple RL circuit serves as integrator that consists of a long superconducting strip line inductance (200pH) and a PdAu on-chip resistor(0.5Ω). The L/R time constant should be considerably larger than the sampling intervals. Each SFQ pulse decreases the input current exactly by the amount of $\Phi_o / L_{feedback}$, indicating the advantage of the RSFQ as an analog quantity with the quantum mechanical accuracy.

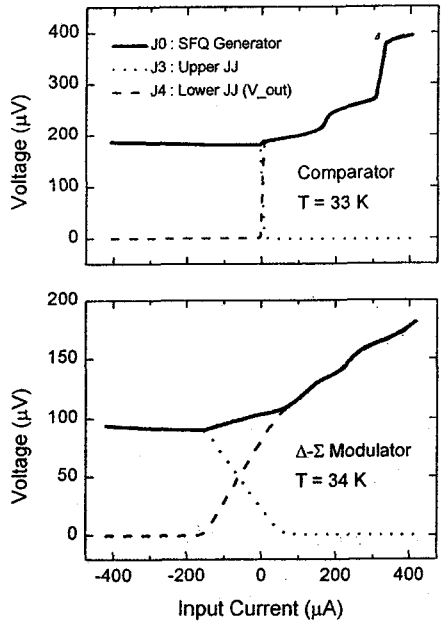


Figure 5 Characteristics of the balanced comparator and the Δ-Σ modulator. The widening of the transition width is the indication of the feedback operation.

3-3. Measurement

To confirm the noise shaping, high-speed measurement is required. But our measuring probe was designed only for dc measurement, hence it has the bandwidth of a few kHz at most. But the effect of the feedback loop can be clearly seen in the dc measurement, as shown in the figure 5. The major change in the current-voltage characteristic is the broadening of the effective transition width ΔI. The output is linear within the transition region, and the slope is independent of the bias current into the comparator. This simply reflects the fact that the delta-sigma modulation doesn't depend strongly on the detailed characteristic of the comparator.

To check the linear response of the modulator, we measured the output signal from a pure sinusoidal input of 19360 Hz. The result is shown in figure 6. The ratio of the signal and the first harmonic was 40 dB, or 5-6 effective bits equivalently[7]. It is still far from useful, but we believe that the noise floor is determined by the measurement setup, and the

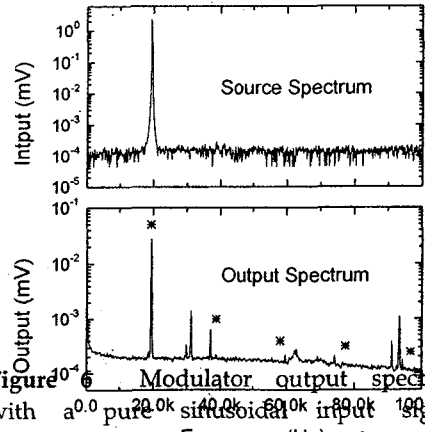
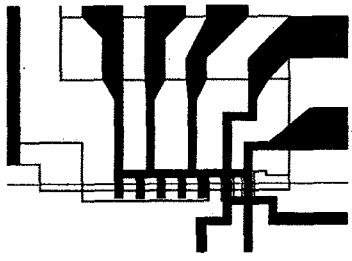


Figure 6 Modulator output spectrum with a pure sinusoidal input signal. Markers are the locations where harmonics will occur. Other peaks are background noise signals. [7]

actual resolution is better.

4. Design of a T Flip-flop

The multilayer bicrystal technology can be readily applied to demonstrate small-scale Josephson devices with ground plane. Since the high-T_c Josephson technology is still primitive, the bicrystal junctions can be used as the first step to prove the possibility of high-T_c Josephson devices. The right strategy we should take might be that we now test several layouts and circuit design with the currently available bicrystal junctions and multilayer, and wait for a breakthrough in the high-T_c Josephson technology. When high quality Josephson junctions become available, then the knowledge learned by the bicrystal circuits becomes quite useful.



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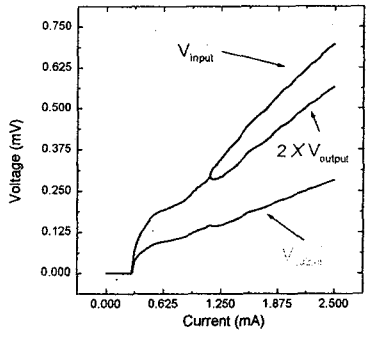

(b)

Figure 7 (a) Design of a T flip-flop with multilayer bicrystal Josephson junctions. (b) Simulation or IV characteristics with optimum circuit parameters

As another application of the multilayer bicrystal Josephson junction technology, a toggle flip-flop (TFF) is designed. Figure 7 shows the layout and simulation result with optimum circuit parameters. Here, the 3-dimensional structure provides flexibility to the single-line bicrystal substrate. A 3-dimensional structure has already suggested using Nb junctions (named as "stacktron")[8], and this will help increasing packing density of the superconducting circuits.

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