Two-Wire ISDN S-Interface Transmission System

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Abstract

In this paper, we suggest a way of implementing ISDN S-Interface through two-wire premises telephone networks instead of using four wires as in the existing ISDN systems. This will help many developing or underdeveloped countries in the world to introduce ISDN services, where they have only two or four wires as in-building telephone networks. We suggest new physical-layer specifications for two-wire S-interface similar to that in ITU-T recommendations I.430 for four-wire systems, design a tranceiver according to the suggested specifications, and implement it using an FPGA We build a test board with the chip on it and succeed in connecting to Internet.

I. Introduction

ISDN is a full-duplex digital communication network on telephone lines with transmission rate of 144kbps for basic rate interface (BRI) and 1.544 – 2.048Mbps for primary rate interface (PRI), through which integrated communication services such as voice, data, image, etc. are provided. ISDN is invented in the early 1980's and commercial services are currently available in some countries. Recently, spreading of internet stimulates the explosive demand for high speed transmission such as ISDN.

The end branches of ISDN networks are composed of the network terminator (NT) and the terminal equipment (TE). The interface between the NT and TE are called S-interface and transmission at the S-interface is through premises (i.e., in-building) telephone networks[1]. The physical-layer standards for the S-interface are described in the ITU-T recommendation I.430[2]. They consider four-wire interconnection between the NT and TE. Two wires are for the transmitter and the other two are for the receiver. Problem arises here because in many developing or undeveloped countries (including Korea), they have only two or four telephone lines in most of home buildings. If conventional analog phones have already occupied two wires, no or only two wires are left for ISDN facilities. The present situation in Korea for example is that the service providers entirely neglect the existing telephone lines inside of the walls and the ISDN subscribers should endure the inconvenience of newly installed four-wire lines crawling on the floors and walls!

We suggest new physical-layer specification which accommodate on the two-wire lines and a tranceiver according to it. We show the experimental results through FPGA implementation of the tranceiver.

II. Tranceiver Design for Two-Wire S-Interface

1. Transmission Model

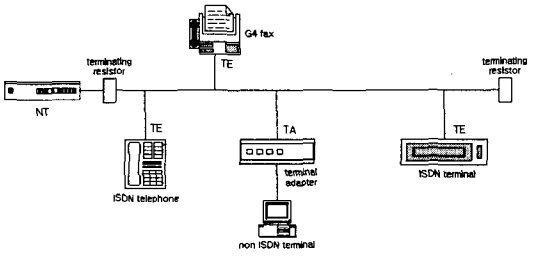

Fig.1 Transmission model.

Two-wire S-interface provides point-to-multipoint interconnection in the short passive bus configuration as shown in Fig.1. Maximum of eight TE's can be connected to the NT through two-wire telephone lines[2]. The length of the passive bus is limited approximately to 50m here instead of around 200m which is the case of conventional

S-interface. Both ends of the bus are impedance-matched by the terminating resistors as shown. Access channels of two-wire S-interface operate exactly the same way as that of four-wire interface. There are two B channels and one D channel (2B+D). They also employ inverse AMI line code[3]. Reference clocks are provided to the NT from the public network side and the TE's recover the data clock and the frame sync from the NT signal.

2. Data Signal Design

The conventional four-wire S-interface achieves the full duplex transmission by using two wires for transmitting signals and two wires for receiving signals. For two-wire systems, this can not be the case. Here, we suggest a kind of time-division duplex (TDD) technique called ping-pong to do the job. The NT and TE signals occupy different portions of a bit interval. Each TE should be able to distinguish signals from other TE's, from NT signal to acquire data clock recovery from the latter. This scheme is valid since there is enough bandwidth for 192kbps transmission in the channel, because we are considering only short passive bus configuration with maximum length of around 50m.

The NT and TE's employ inverse AMI line code. The different pulse width of the NT and TE signals make it possible for a TE to distinguish one from the other. Fig.2 shows the signals at the two-wire S-interface. The shorter-duration pulse is the NT signal and the longer-duration one is the TE signal. The shaded area is due to the different delay times of the TE signals from different TE's. The NT should sample the TE signals in the interval where the signals from all the TE's are stabilized. It is indicated as NT sampling interval (T_S) in Fig.2. The pulse width of the NT and TE signals are also related with the transmission distance. From Fig.2, it can be shown that

$$T_{RTD} \le T - (T_{NT} + T_{TE} + 2T_G) \qquad (1)$$

and

$$T_{RTD} \le T_{TE} - T_S \qquad (2)$$

where

- T : bit interval ;
- T_{RTD} : round trip delay ;
- T_{NT} : NT signal pulse width ;
- T_{TE} : TE signal pulse width ;
- T_G : guard interval ;
- T_S : NT sampling interval.

It is seen from Eqs.(1) and (2) that to increase the T_{RTD} (i.e., the transmission distance), T_{NT} should be decreased and T_{TE} should be increased. The clock jitter of the TE limits the decrease of T_{NT}. Eq.(2) indicates that T_{RTD} is always less than T_{TE}, meaning the limitation of transmission distance. It is actually true that in our scheme the transmission distance is not limited by attenuation of the channel but by T_{RTD} constrained as indicated in Eqs.(1) and (2). For the same reason, it also should be revealed that our scheme is no longer valid at higher data rates such as for PRI.

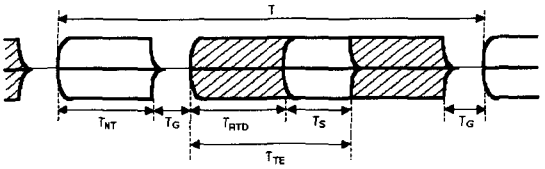

Fig.2 Signals at two-wire S-interface.

3. Synchronization

There are two kinds of synchronization which should be considered in ISDN S-interface. One is the data clock recovery and the other is the frame synchronization. The frame structure for two-wire S-interface is the exactly the same as that for four-wire system and the procedure for frame synchronization for both systems are exactly the same. One important difference in data clock recovery between the two systems is that in two-wire systems, there co-exist both the NT and TE signals in a single channel. Since each TE should obtain the clock information from the NT signal, it should be able to distinguish the NT signal from that of the other TE's. The pulse width of the NT signal is shorter than that of the TE signal. Each TE searches out the NT signal using two edge detection windows and the pulse-width difference of the two signals. After the NT signal is found out, the data clock is synchronized to it using DPLL. The TE inputs only the NT signal to the phase detector using the input window and interference effects from other TE signals and noise can be reduced[4].

III. Tranceiver Structure

Fig.3 shows the basic structure of the two-wire S-interface tranceiver. The structure is similar to that in SBCX chip (PEB2081) from Siemens. In Fig.3, the analog parts are the hybrid, driver (Tx), and comparators (Rx). The other parts are digital. The digital parts are implemented using FPGA (Altera). The tranceiver operates either in NT mode or in TE mode. The functions of major blocks are described in the followings.

O AMI coder

Two-wire S-interface employs the inverse AMI code as the line code, just like the conventional four-wire system. The symbol rate for S-interface is 192kbps and there are five kinds of frame types. They are INFO0 (no signal), INFO1 and INFO3 (for TE), and INFO2 and INFO4 (for

NT), respectively. The AMI coder produces inverse AMI signals for B1, B2, and D channel data in the transmit buffer according to the coding rule and the relevant frame type.

O AMI decoder

The AMI docoder decodes and separates each channel data from one another from the received signal. It transfers the channel data and frame type to the S-interface controller in the higher layer and also supplies the frame sync information to the frame synchronization block.

O D channel controller

This controls the D channel access of multiple TE's. For NT mode, it only retransmits the D channel data in the receive frames through the ECHO channel in the transmit frames. For TE mode, in operates according to the D channel access algorithm described in ITU-T recommendation I.430.

O S activation/deactivation detect

It determines the activation or deactivation of the transceiver by detecting the activation/deactivation state of the S-interface.

O RXPLL

This performs the task of data clock recovery in TE mode operation. Since, according to I.430, there are at least four 0's in a S-interface frame, it detects at least four NT pulses using the edge detection windows in a frame. In case that it fails to search NT pulses for predetermined period of time, it shifts the edge detection windows by one clock period and tries again. After the NT signal is found out, the data clock is recovered by DPLL.

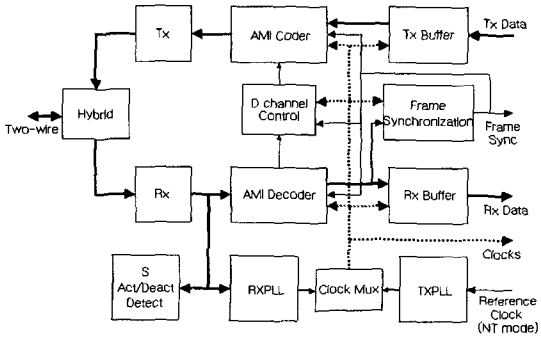

Fig.3 Tranceiver structure.

O TXPLL

The clock is supplied to TXPLL from the public network side in NT mode operation.

O Frame synchronization

It performs the frame synchronization by recognizing the coding rule violations described in I.430.

IV. Experimental Results

The tranceiver is implemented using FPGA from Altera. The two-wire channel used in the experiment is a telephone line with the length of 50m and with no bridge taps. One tranceiver in one end generates both the NT and TE signals and one in the other end synchronizes its data clock to the received NT signal. Fig.4 shows the result. The upper waveform is the input signal to the TE and there co-exist both the NT and TE signals in it as is seen. The shorter-duration pulses are the NT signal and the longer-duration ones consist in the TE signal. The lower waveform represents the TE data clock signal synchronized to the input NT signal. The delay because of the 50m length of the channel can be seen in Fig.4.

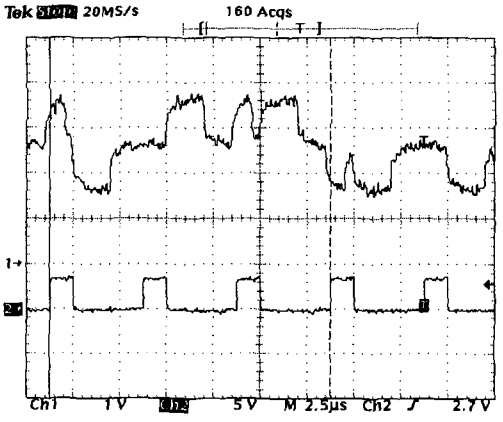

Fig.4 Experimental result for data clock recovery.

Fig.5 shows the experimental result for frame synchronization. One frame interval is between two successive "F" bits. The upper waveform is the received NT pulses and the lower waveform is the synchronized frame clock. In the upper waveform, the inverse AMI coding rule violation can be seen at the "F" bit and at the first "0" bit after "L" bit just as described in I.430.

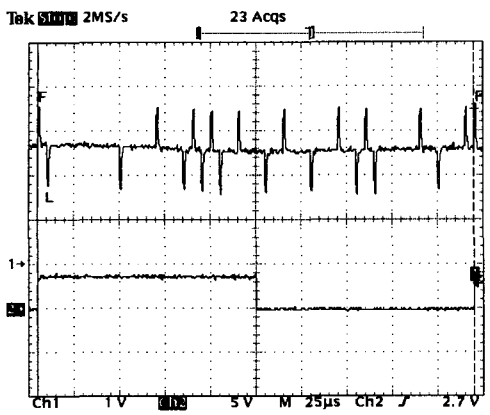

Fig.5 Experimental result for frame synchronization.

V. Conclusions

This paper suggests a new S-interface technology to provide ISDN services through two-wire premises telephone networks. We suggest basic model for two-wire S-interface transmission and method of full-duplexing on a single physical medium using an TDD called ping-pong for point-to-multipoint interconnection. The tranceiver structure is suggested and implemented through FPGA. The experimental results for the most important functional blocks, data clock recovery and frame synchronization, are shown.

The suggested technology is brand new as far as we know and will contribute to activate the spreading of ISDN services, especially in such countries that have unfavorable telephone network facilities. The suggested two-wire S-interface system employs most of the specifications for the four-wire system. It modifies only the tranceiver part of the conventional four-wire system. The entire S-interface chip is implemented using FPGA by our research group. We build a test board and insert it in a PC rack. We succeed in connecting to the Internet using the test board and two-wire telephone lines.

Acknowledgement

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References

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