High Integration Packaging Technology for RF Application

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Outline

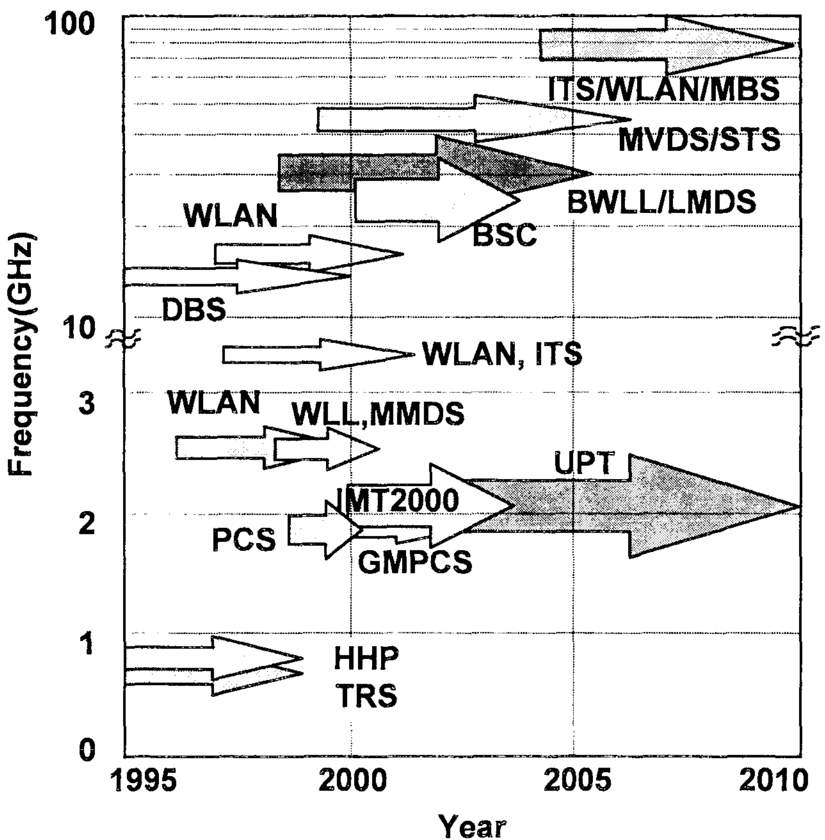
- **Overview of RF ICs and Packaging Technology**
  - **Wireless RF ICs Trends**
  - **Features of RF Packaging**

- **Main Technologies in RF**
  - **Flip Chip, CSP and MCM**
  - **Passive Component Integration**

- **Examples of Research Results**
  - **WLP-CSP Development**
  - **Integrated L, R, C**

- **Summary**

Wireless Communications Revolution



- Service Merging
  - Wire and Wireless Communications
  - Communication and Broadcast

- Mobile Multimedia Services
  - Anytime, Anywhere
  - All of service ; voice, data, video

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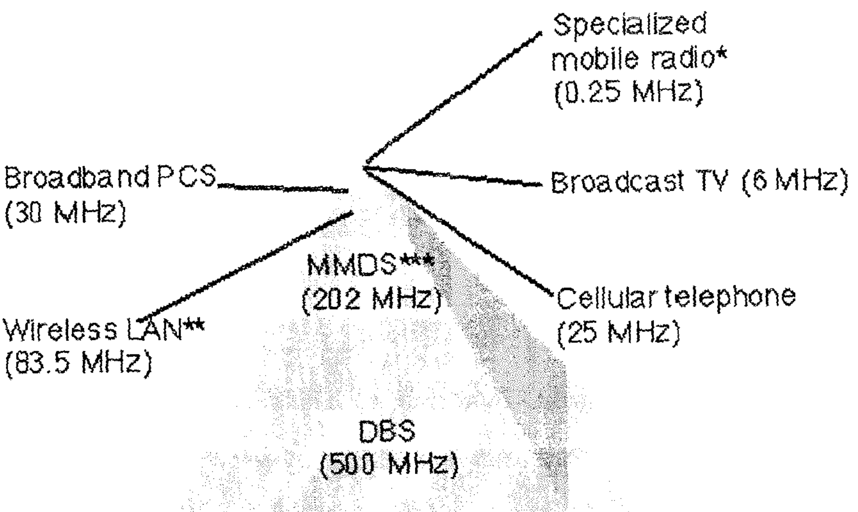
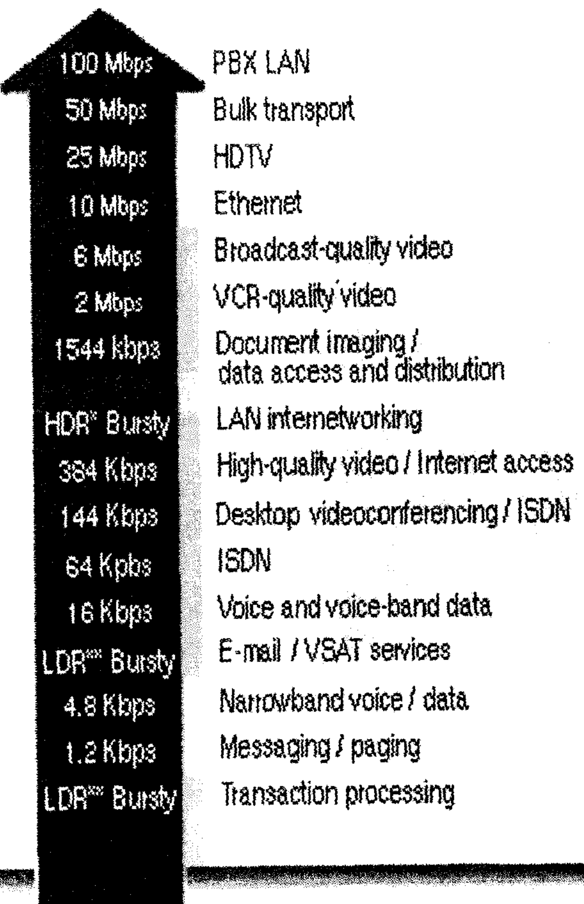
Bandwidth and Data Rate





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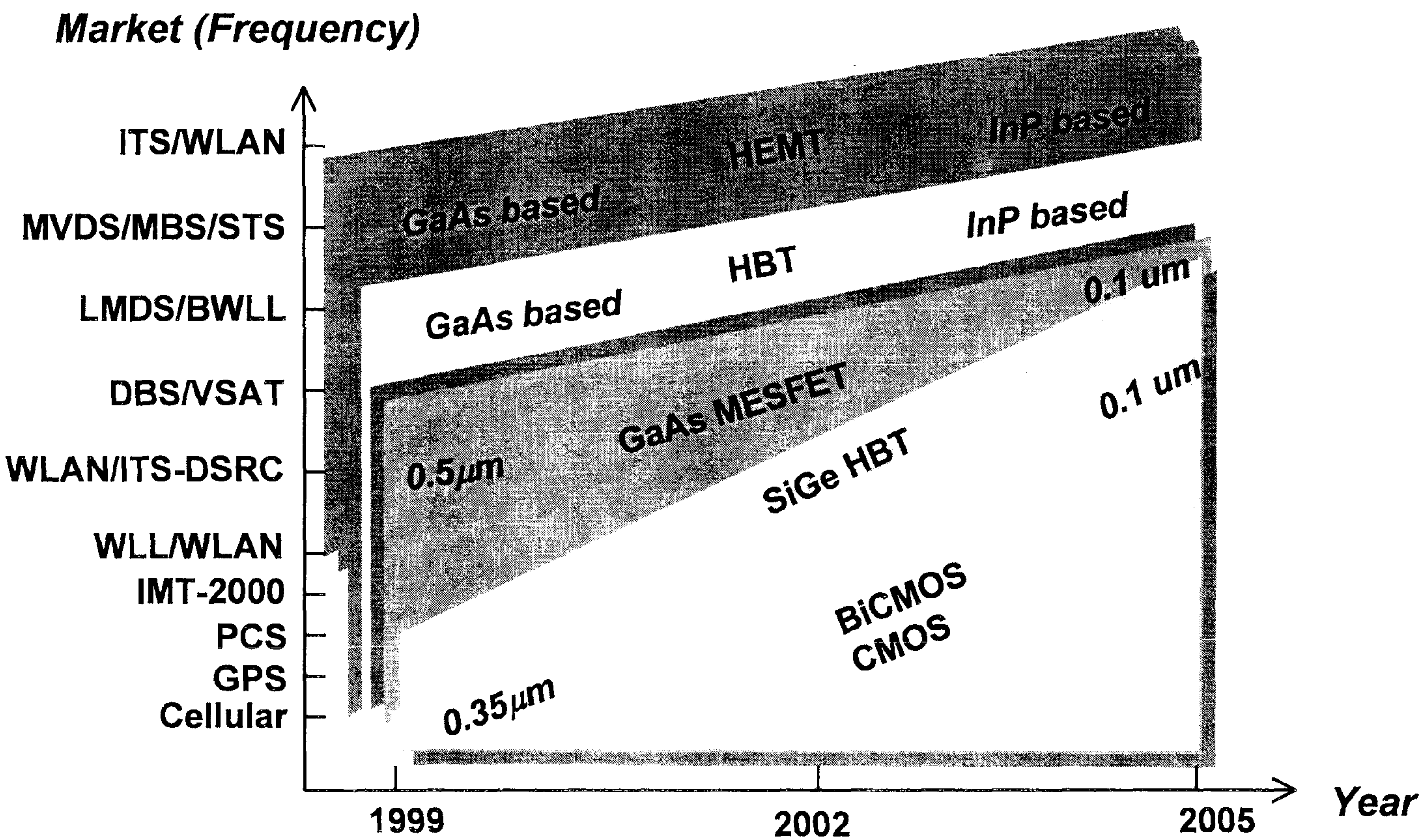
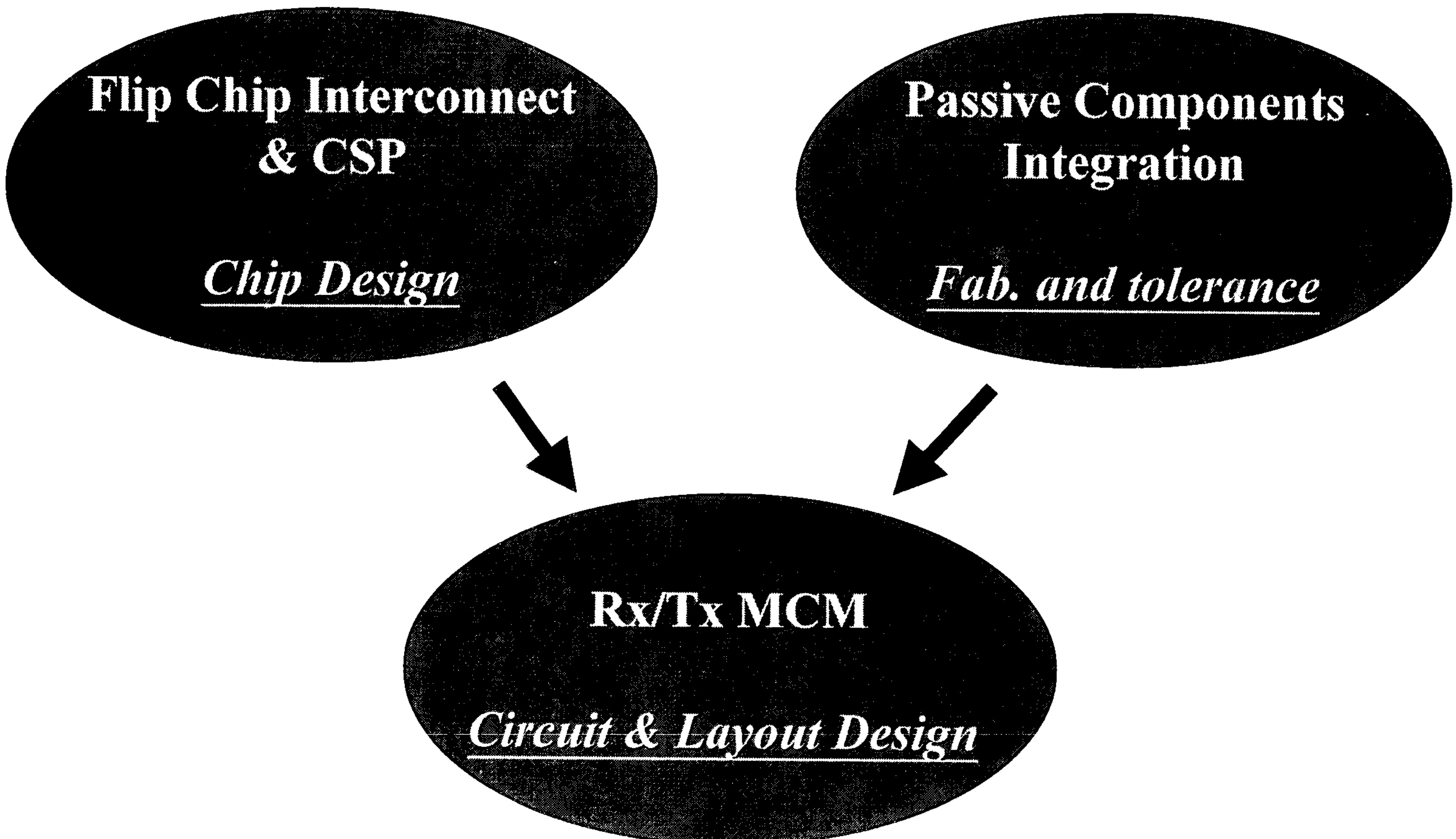
Trends of RF Device Technology



Discrimination between RF and Digital High-Speed Systems

	RF	Digital
Net Density	low	very high
Data Exchange	cascaded signal R_x -> IF -> Base Band Base Band -> IF -> T_x	synchronized data simultaneous switching
Signal Integrity	frequency domain approach impedance matching insertion loss, return loss network analysis	time domain approach timing (Prop. delay) SSN (low inductance) SPICE & TDR analysis
Passive	many L, R, C for circuits and matching	not so many de-coupling C termination R
package I/O	typically < 20	several hundreds

Emerging Streams in RF Packaging Technology



Driving Forces : Performance, Miniaturization, Low Cost

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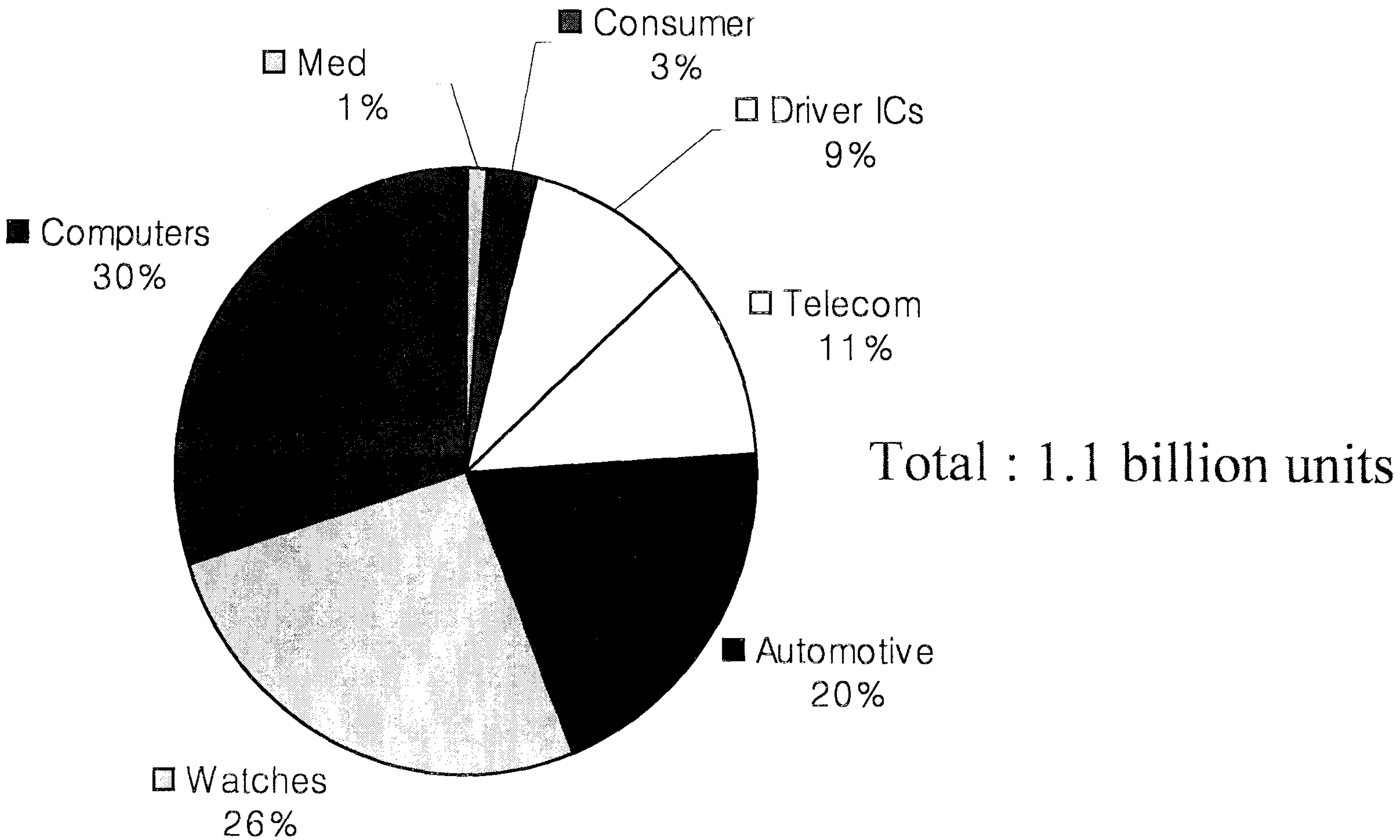
Flip Chip Market Forecast in 2000



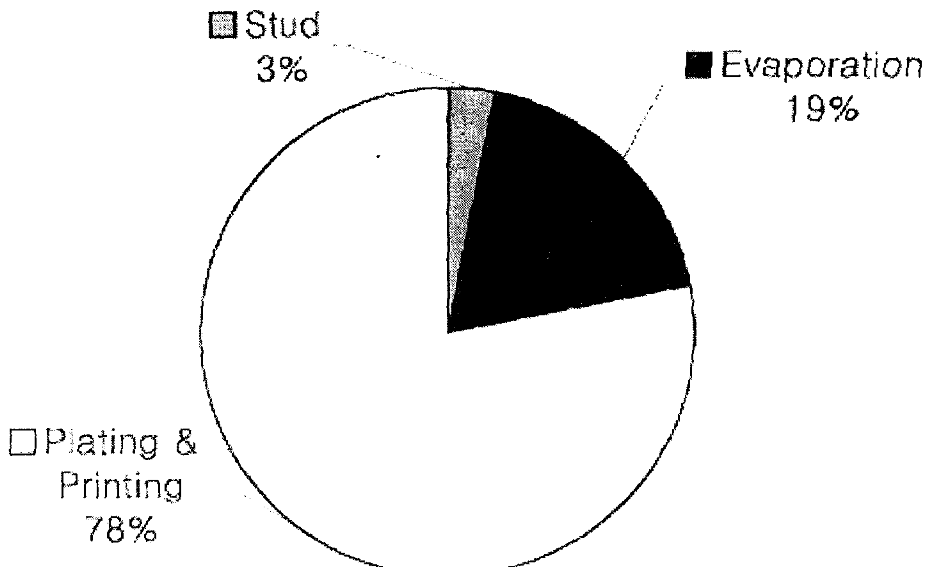
Total : 1.1 billion units

Source : Advancing Microelectronics,1999

Need of Flip Chip for RF ICs

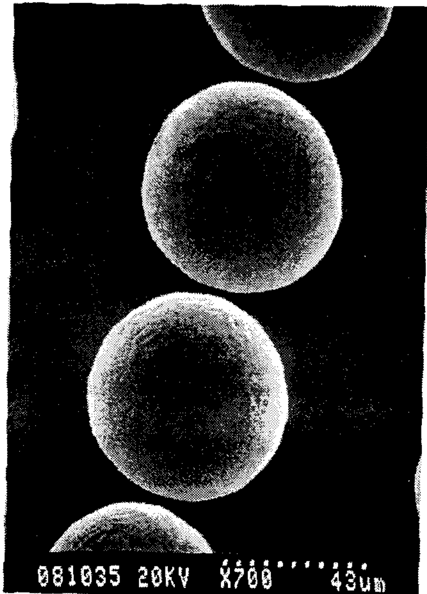
- Better electrical performance
  - Short interconnect length and so low inductance
  - Low performance loss
- Easy to miniaturize RF module as a die form
- Not need wafer back-lapping
  - Higher process yield and so lower cost
- Better thermal dissipation
- Self-alignment
- Less sensitivity on solder joint reliability due to small die size

Bump Formation



Source : Advancing Microelectronics,1999

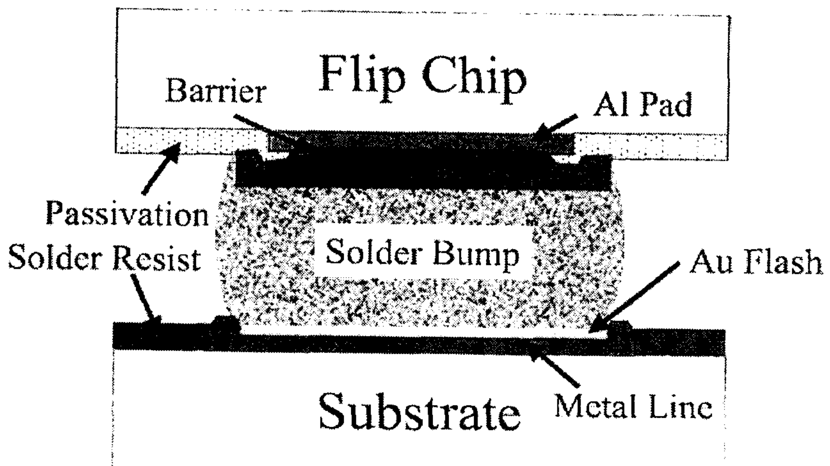
(a) Portion of bump fabrication method



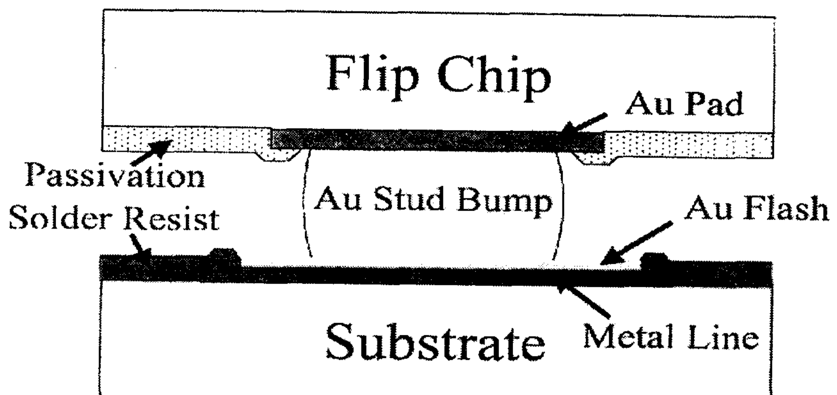
(b) Example of solder bump

Note : Au stud bump is mostly used due to easy fabrication at research step

Methodology of Flip Chip Interconnection



(a) Solder Bump



(b) Au Stud Bump

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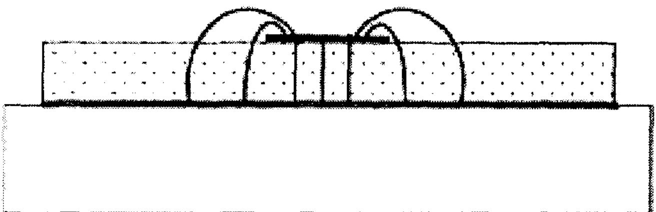
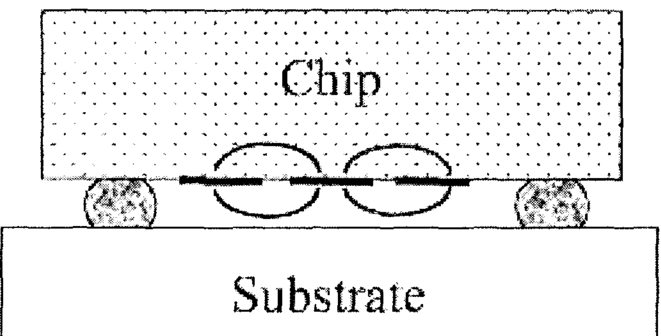
Electrical Field Approximation for RF IC Design

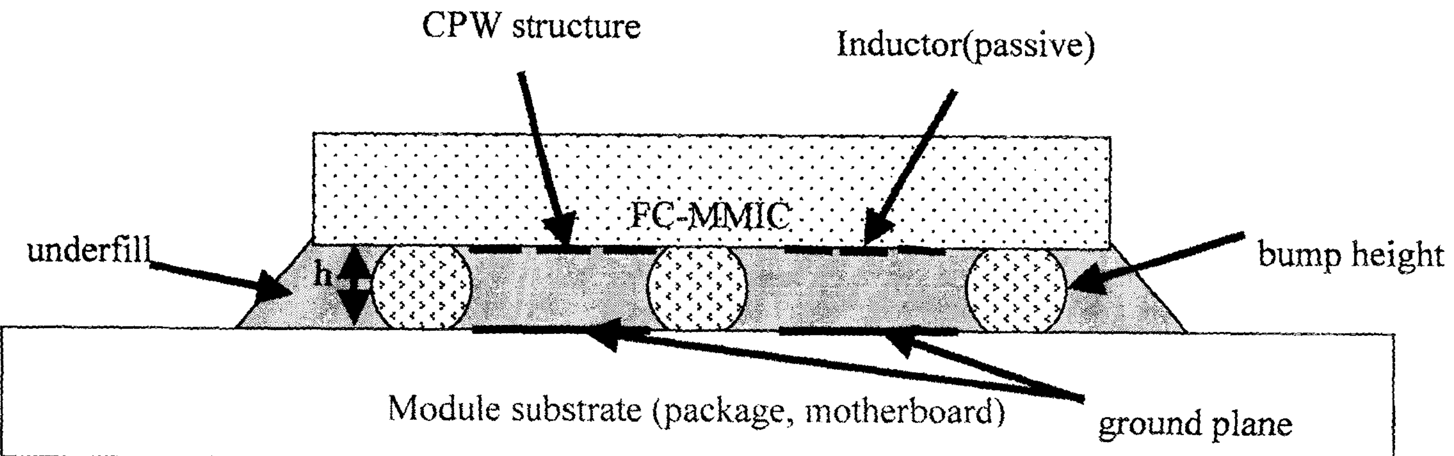


(a) Microstrip



(b) Coplanar Wave Guide

Key Technologies in RF Flip Chip



- CPW transmission line design
  - width/space of GSG, line thickness, line mat'l
- Structural factors on the performance of CPW
  - substrate structure, bump height, underfill, backside metallization
- Thermal resistance
- T/C reliability

Examples of RF Flip Chips

Company	Function	Technology	freq.	Features
Hughes '97	- Driver Amp. - VCO - Static Fre. Divider	- SiGe - Bipolar	Ku-band	- Polyimide microstrip MMICs ; Top layer : ground plane ; Si-based devices
	- MIC Amp - Fre. Divider	- InP based HEMT	Ku-band	- Flip-chip MICs ; solder bump
NEC '98	- LNA	- CPW MMIC - GaAs	- 30 GHz - 60 GHz	- Co-planar waveguide line - Bare chip thick : 150 um - 20 um high Au bump : Thermal compression - with or without underfill - Flip Chip on Al2O3 substrate ; Performance Test, S-Parameter
Fujitsu '98	- Automotive Radars chipset	- 0.15 um InGaP/ InGaAs HEMT	- 76 GHz	- chipset consisting of 76GHz Amp, mixer, SPDT switches, 38/76GHz doubler, 38GHz VCO, and 38GHz buffer amp. - Co-planar waveguide MMIC - Co-planar waveguide Al2O3 substrate (Sn pad) - 20 um high Au bump, d=40 um
NEC '98	- 3 stage Amp.	- GaAs	- W-band - 77 GHz	- Co-planar waveguide line - Bare chip thick : 150 um without metal - 20 um high Au bump : Thermal compression - with or without underfill - Flip Chip on Al2O3 substrate(CPW)

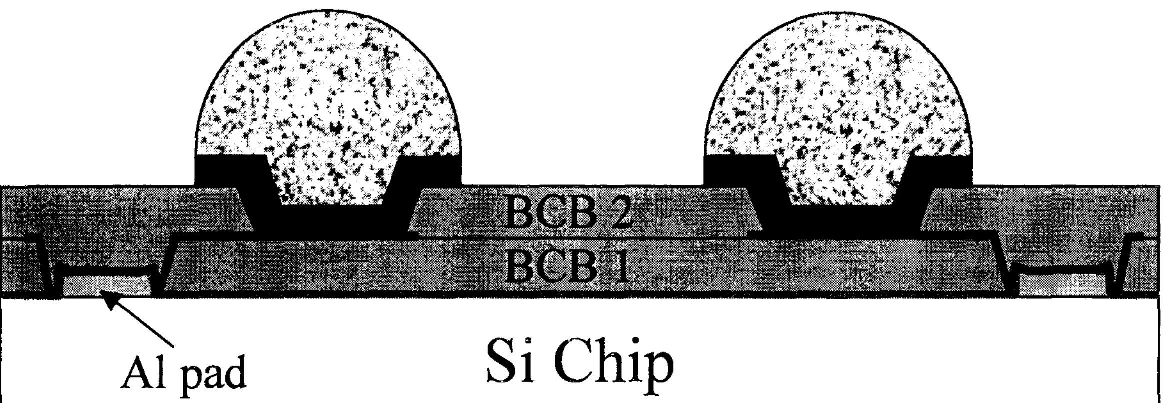
Examples of RF Flip Chips (continued)

Company	Function	Technology	*freq.*	Features
Fujitsu '98	- 2 stage Amp.	- 0.15 um InGaP/ InGaAs HEMT	- W-band (79 GHz)	- Co-planar waveguide MMIC ; 600 um thick, 2 um thick Au line - Co-planar waveguide Al2O3 substrate (Sn pad) - 20 um high Au bump, d=40 um (Au/AuSn) - Z_o measurements of transmission line (EM anal.)
Huges	- HPA	- 0.25 um PHEMT	- X-Band	- Bump : Ag plating, h=100 um, d= 150 um - 40 % enhanced thermal performance - 40 % reduced cost
GEC Caswell '98	- PA, VCO - for HIPERLAN	- GaAs MMIC - Via provessing - Flip Chip on MCM-D	- 5.2 GHz	- At FCB, GND plane must be removed under Inductor of FC-MMIC - Solder bump - MCM assembled with 17 mm BGA
Siemens '98	- CPW line - Filters - PA	- Poly Diamond Substrate - GaAs MMIC PHEMT	- 1 ~ 120 GHz - 28 GHz	- PE-CVD processing Diamond wafer ; $\tan\delta$ as low as $4X10^{-5}$, $\varepsilon_r = 5.7 \pm 0.05$ at 145 GHz - Electrical characterization of CPW - Flip chip on diamond - Au bump without back thinning
Raytheon '98	- ETL Amp.	- GaAs MMIC - BeO μ-BGA	- 10 GHz	- not thinned (635um) - 25 um PI, RF GND plane(top) - 10 mil solder ball BeO μ-BGA
Raytheon '98	- ETL Amp.	- GaAs MMIC - pHEMT - BeO μ-BGA	- 11.5 GHz	- not thinned (635um) - 25 um PI, RF GND plane(top) shielding - Z-axis chip adhesive interconnect - 10 mil solder ball BeO μ-BGA

Examples of RF Flip Chips (continued)

Company	Function	Technology	*freq.*	Features
Fraunhofer Institute '97	- CPW line	- GaAs	- 10 ~ 120 GHz	-Difference of Electrical results between CPW line of Flip chip and CBCPW(conductor backing)
GM Huges '95	- T/R Module	- CWP based circuitry - MESFET		- Ag plated bumps for electrical interconnect ; 75 um ~ 90 um high - T- shaped thermal bump
Univ. of Colorado at Boulder '98	- Characterization on CWP line and its RF performance	- GaAs - 50 Ω CWP line		- Solder joint reliability and performance degradation with or without underfill ; d=150 um, h=70um, die thick=635um - GaAs on ceramic or Duroid substrate - Ag-bump for RF Performance ; h=75 um, d=150 m, - Au(5um)/Ti(0.02um)/ceramic - Additional degradation due to underfill was less than –1dB
Sharp '98	- GSM class V PA	- AlGaAs/GaAs HBT	-900 MHz	- FCB on Al2O3 - Low profile package (6.35X6.35X1.05 mm3)
Univ. of Massachusetts	- Modeling			- Both coplanar and microstrip chips are circuit modeled and their results are compared.
Univ. of Michigan	- Low noise Amp.	- Inp HEMP	- K-band ; 20 GHz	- Si micromachined conformal package

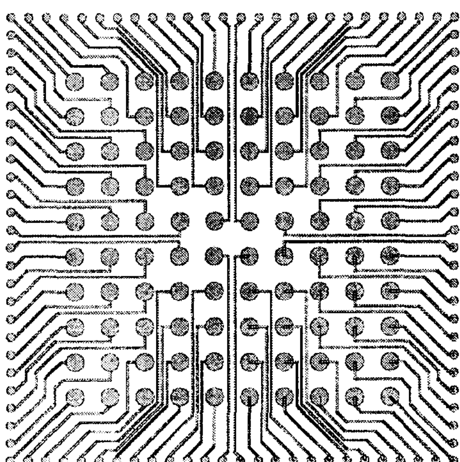
Example of WLP-CSP



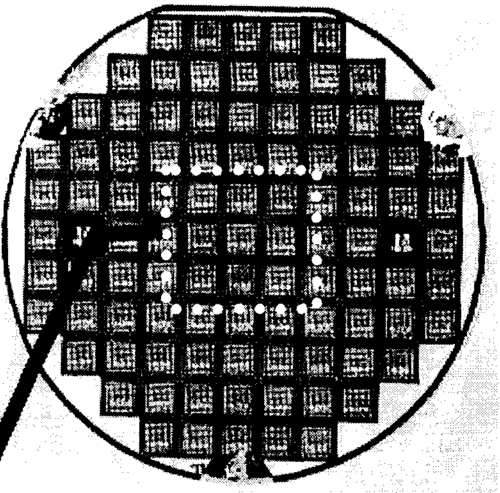
Chip Size	10 X 10 mm^2
Chip Passivation	SiO_2 (0.8 μm)
Dielectric Thickness	7 μm
Conductor	Plated Cu 3 μm thick
UBM	Plated Cu (5 μm)/ Sputtered Cu(0.3 μm/ Sputtered Ti(0.1μm)
Solder	Eutectic Solder

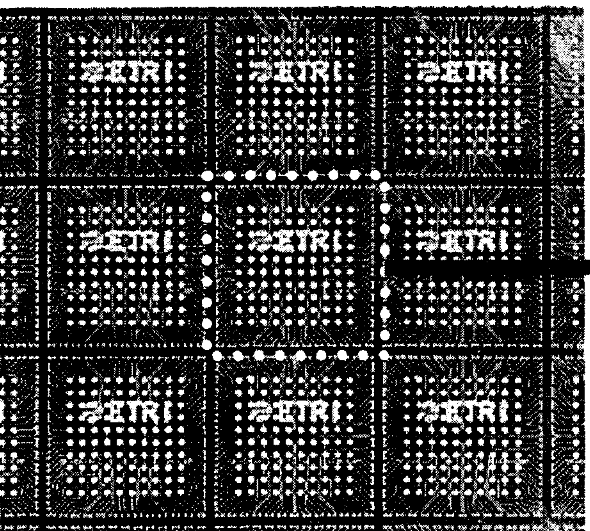
Structure and Features of WLP-CSP

	Vehicle Chip	WLP
Dimension	10 X 10 X 0.63 mm^3	10 X 10 X 0.63 mm^3
I/O Configuration	peripheral bond pad (25 X 4 = 100)	area array pad (10 X 10 = 100)
I/O Pitch	300 μm	750 μm



Example of WLP-CSP





Passive Component Integration

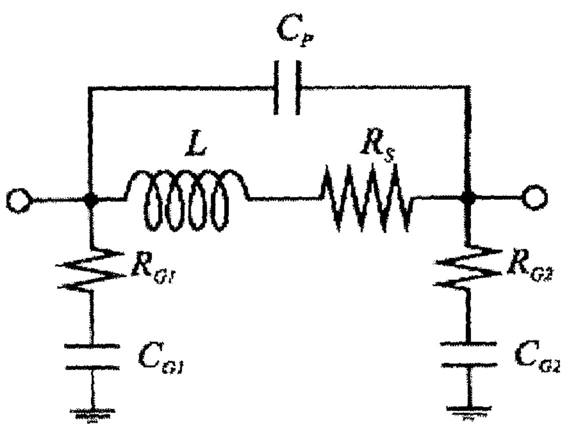
- Ratio of passive to active devices is greater than 15:1
- 100 % Discrete in 1996 -> 70 % Integration in 2004
- The demands of integral passive components are driven by performance, either the reduction of electrical parasitic or miniaturization of system footprint
- On-chip : cost-up, but MCM : cost-down
- MCM-L : only lower cost, MCM-D(Si) : highest integration

Typical Material Systems

	MCM-D	MCM-C	MCM-L
R	NiCr, CrSi, Ta_2N	RuO_3, Ta_2O_5	not proper
L	Cu, Al	Ag, Cu ; LTCC	Cu
C	Ta_xO_y, $BaTiO_x$, SiN_x	Silicates, Titanates	not proper

Design Factors of Integrated L

Device property	Key determinants
Inductance (H)	line width, space, thickness, inner diameter, numbers of turn
tolerance (%)	width and thickness variation
Q	metal thickness, width
self-resonant frequency	inductor area, ε_r of substrate
series R_s	metal thickness, width, total length
parallel R_p	line space, area, ε_r of substrate and encap.
L_s	electrode geometry
R_g	substrate conductivity
C_g	area, separation from ground plane, ε_r of substrat

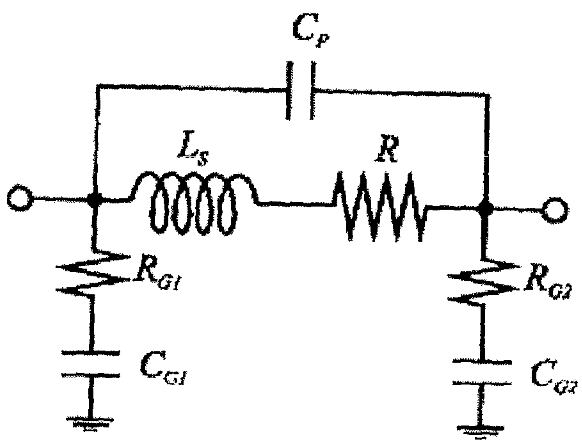


$$Q = \frac{Im(Z_{in})}{Re(Z_{in} - 50)} \quad at \quad 2 \quad port$$

$$where, \quad Z_{in} = \frac{50(S_{11}+1)}{1-S_{11}}$$

Design Factors of Integrated R

Device property	Key determinants
Resistance (Ω)	R_{sh}, width, length
TCR (ppm/°C)	resistor material ~ order of 100 ppm/°C
tolerance (%)	film thickness, pattern width variation
L_s	resistor length, width, thickness
C_p	resistor area, ε_r of substrate and encap.
R_g	substrate conductivity
C_g	separation from ground plane, ε_r of substrate



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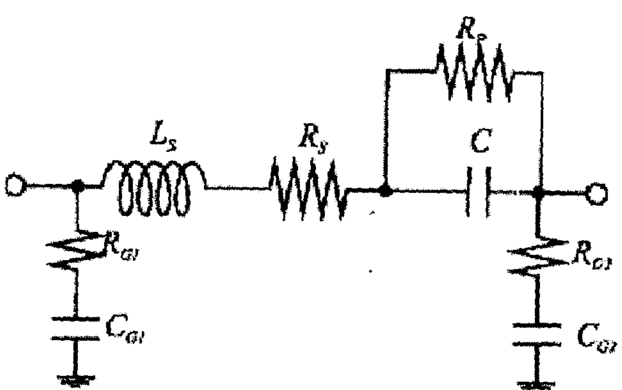
Design Factors of Integrated C

Device property	Key determinants
Capacitance (F)	dielectric constant, thickness, area
tolerance (%)	thickness variation
Q	dielectric loss tangent, electrode mat'l and geome
self-resonant frequency	capacitor area, aspect ratio
series R_s	electrode mat'l and geometry
parallel R_p	dielectric loss tangent
L_s	electrode geometry
R_g	substrate conductivity
C_g	area, separation from ground plane, ε_r of substrat



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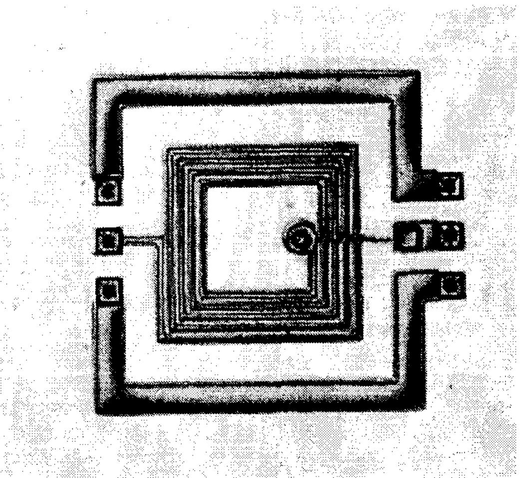
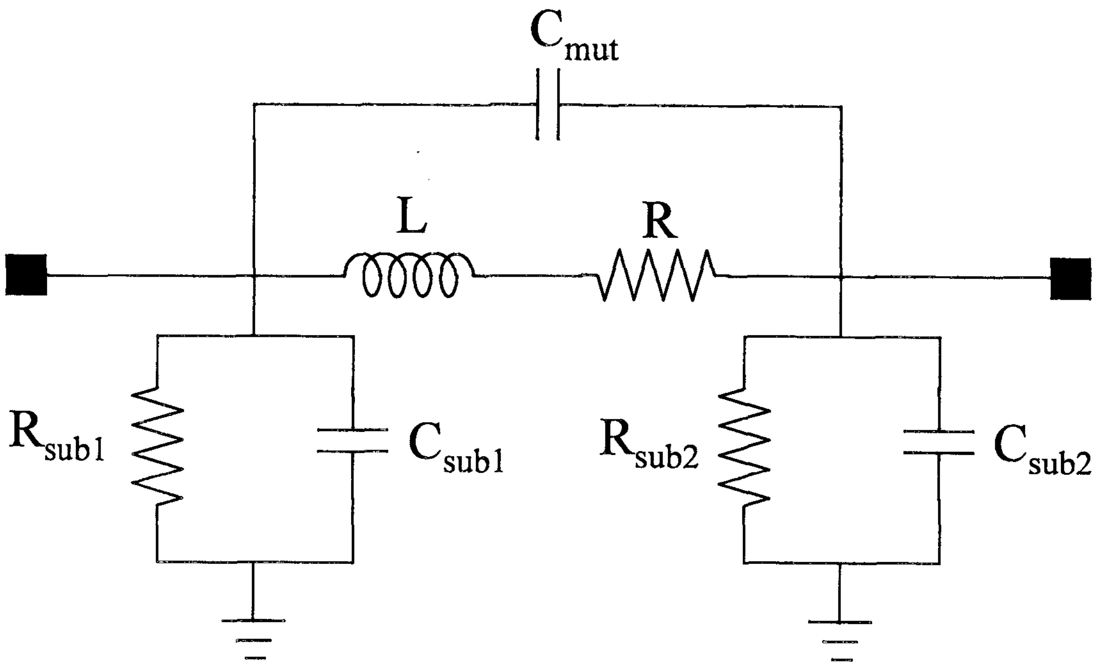
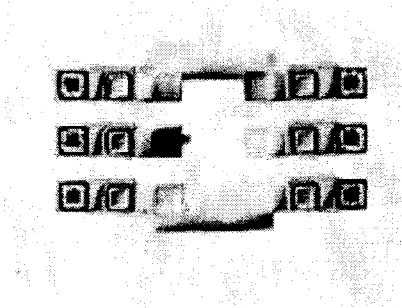
Examples of Integrated L in MCM-D





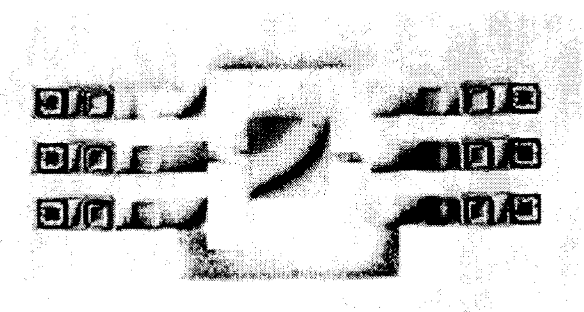
- Cu/BCB multilayer
- Q_{max} = 10.8 at 1.1 GHz (40/20/150/4), L = 5.25 nH

Example of Integrated R and C



(a) Resistor

- NiCr = 20 Ω/□
- Resistor Range : 20 ~ 200 Ω



(b) Capacitor

- Dielectric : Si_3N_4 ($\varepsilon_r \cong 7 \sim 8$)
- Capacitor Range : 20 pF ~ 1 nF

Summary

- Interconnect
  - Wire bonding -> Flip chip interconnect

    ; At research step, Au stud bump bonding seems to be more proper
- Package
  - Plastic package -> Z_o controlled land grid package
  - Flip Chip will be used for RF ICs and CSP for digital ICs
  - RF MCM comprised of bare active devices and integrated passive components
  - Electrical design skills are much more required in RF packaging
- Passive Component
  - discrete -> integrated
  - Both of size and numbers of passive components must be reduced