Characteristics of Lead Frame Chip Scale Package (LF-CSP)

Memory R&D Division

HYUNDAI MicroElectronics

The Semiconductor Group of Hyundai Electronics Industries Co., Ltd

Dec. 15. 1999

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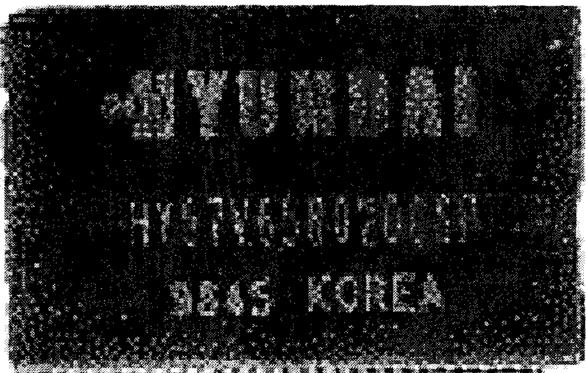
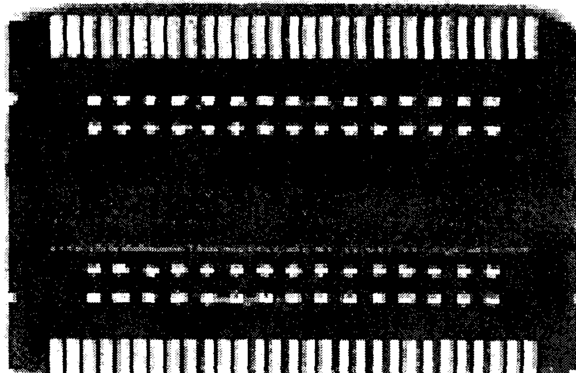
Package General

- Application Device : Memory 60 I/O
- Package Thickness : 1.17mm - Including Solder Ball Height
- Lead Frame : Cu Alloy, Thickness 0.15 mm (6 mil)
- Solder Ball Size : 0.45 mm
- Ball Pitch : 0.8mm
- Solder Ball Composition : 62Sn-36Pb-2Ag

LF-CSP Package Outline

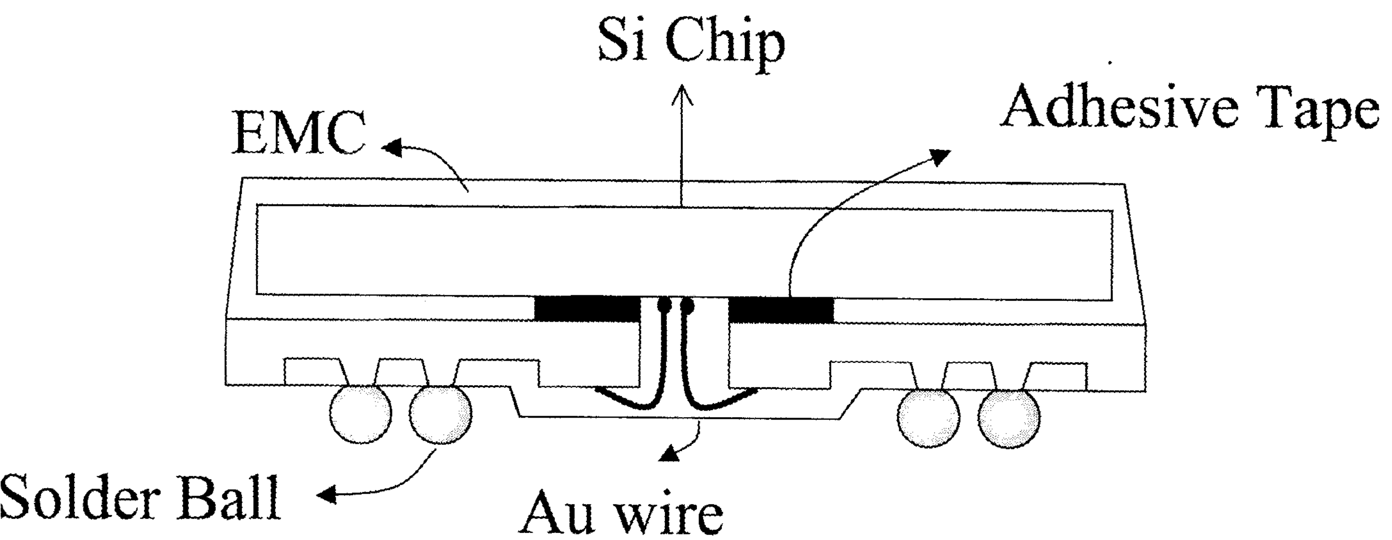


<Top View>



<Bottom View>

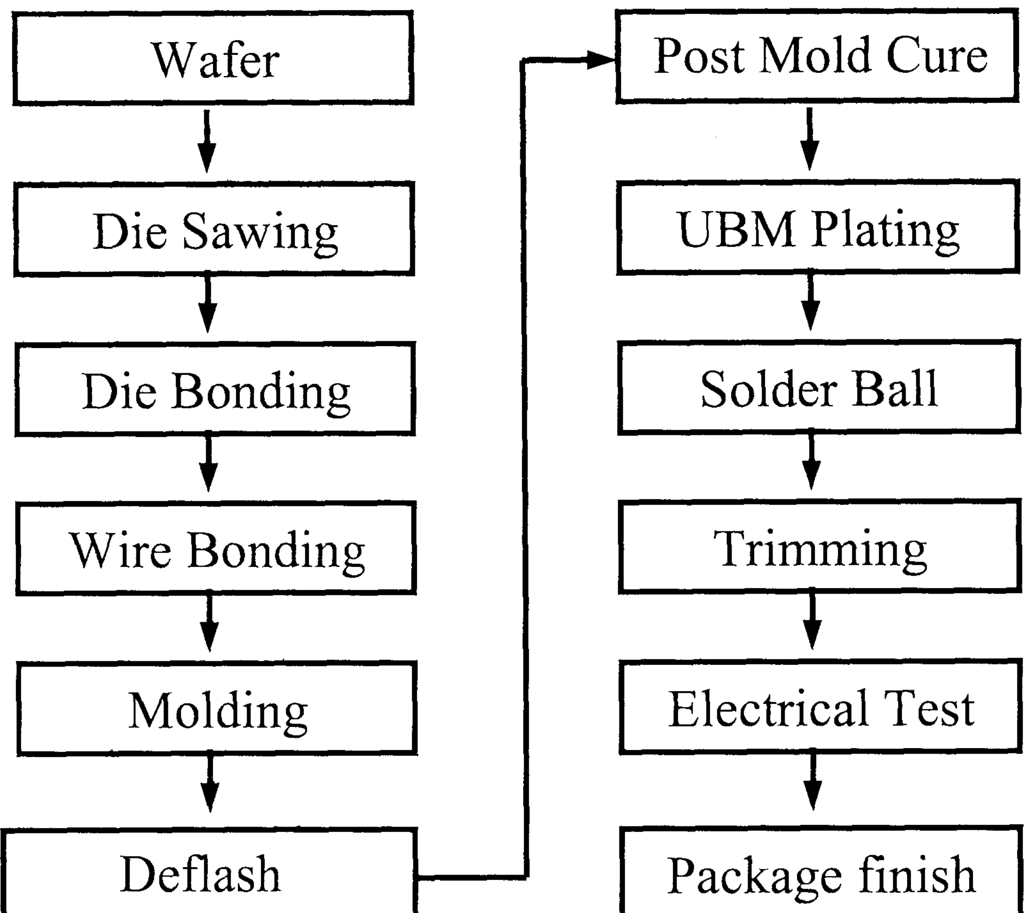
Schematic of LF-CSP



Assembly Key Technologies in LF-CSP

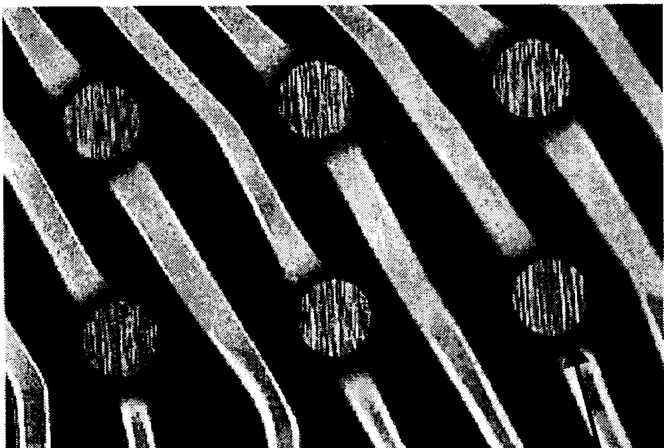
- Half-Etched Lead Frame
- Molding Process
- Deflash Technique
- UBM Technology for Higher Solder Joint Reliability

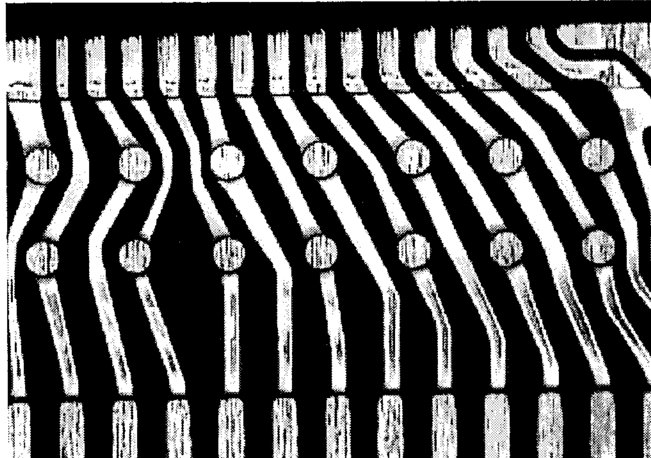
Manufacturing Process



Lead Frame Preparation

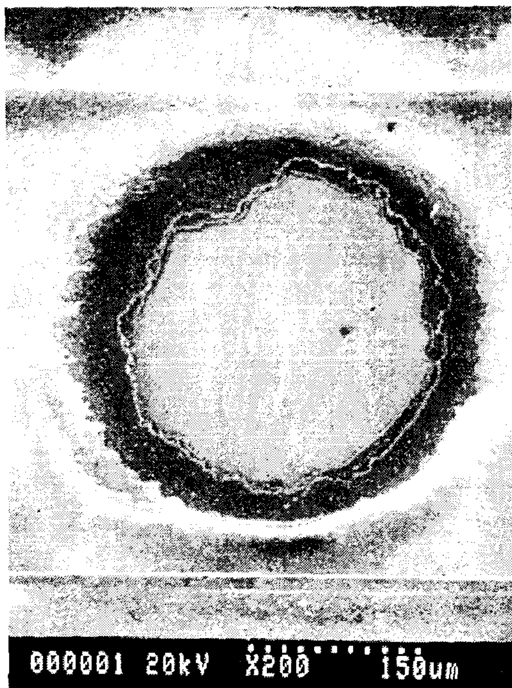
- Cu Alloy Lead Frame with Half-Etched



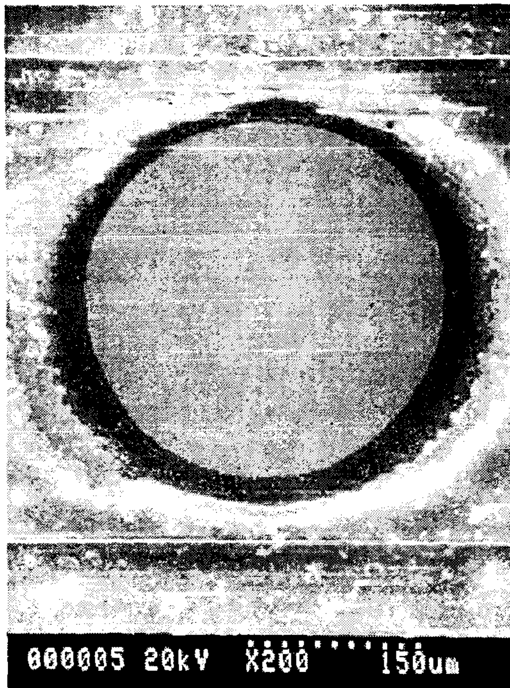


Ball Land

Deflash Technique



< *Before Deflash* >



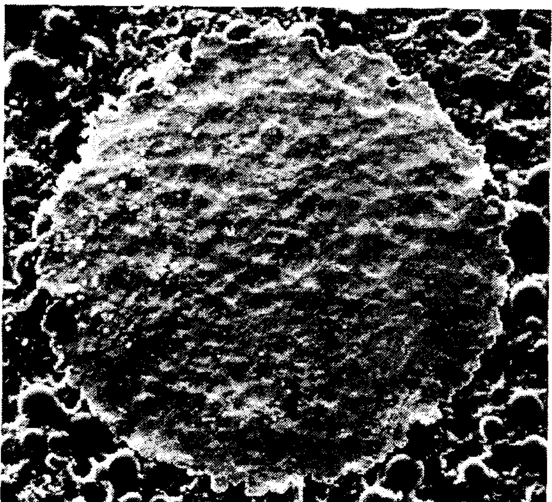
< *After Deflash* >

Deflash Step

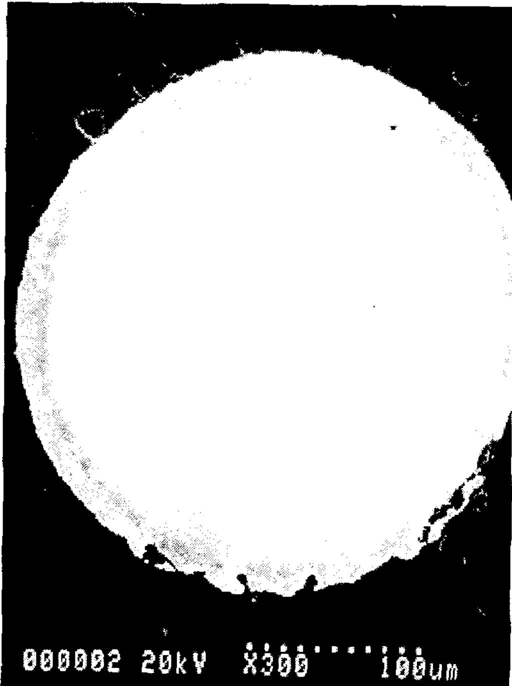
i) Chemical Treatment

ii) Water Jet Deflash

UBM - Electroplating of Ni and Sn-Pb



< After Ni plating >



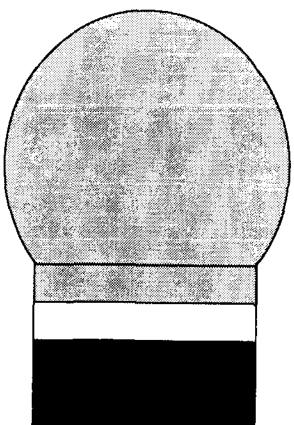
< After Sn-Pb plating >

UBM (Under Bump Metallurgy) System

Ni/Sn-10Pb two layers system

Ni : Cu diffusion barrier layer

Sn-10Pb : wettable layer



Sn-36Pb-2Ag Solder Ball

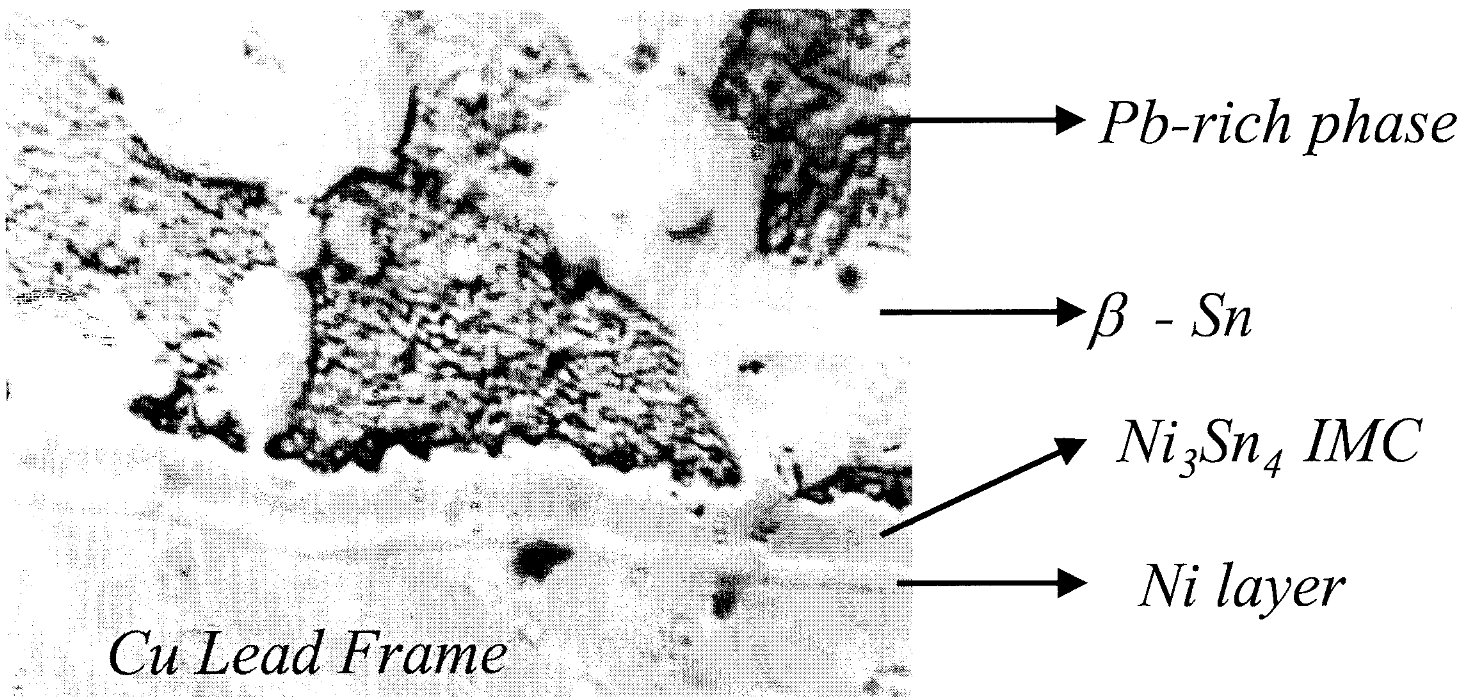
Sn-10Pb*

Ni

Cu Lead Frame

* *Sn-10Pb layer was dissolved into solder after solder ball attachment.*

Interfacial Reaction Between Solder and Ni layer



Pb-rich phase

β - Sn

Ni_3Sn_4 IMC

Ni layer

Epoxy Molding Compound Property

Item	A	B	C	D	E	F	G
Epoxy resin	OCN	OCN	OCN+BP	OCN	OCN	BP	OCN+BP
Filler content	82	82	85	75	77	89	80
α1 (ppm/℃)	13	13	12	16	14	9	13
α2 (ppm/℃)	47	50	50	60	60	35	57
Flexural Modulus	2000	1900	2100	1550	1100	2600	1600

Filler content = wt%, Flexural Modulus = kg/㎟

Temp. Cycle Test for EMC

Item	A	B	C	D	E	F	G
Precondition	0/5	0/5	0/5	0/5	0/5	0/5	0/5
T/C 200	5/5	5/5	0/5	4/4	3/3	0/5	5/5
T/C 500	-	-	0/5	-	-	0/5	-

. Type C,F,G(Biphenyl epoxy resin content) need bake at 5min before deflash process

. Precondition : 125℃/24hrs Bake, 85℃/85% 168hrs, IR 2cycle

. Temp. Cycle : - 65℃ ~ 150℃ (Ramp : 5min, Dwell : 10min)

. Crack Mode : Outer Ball Land Area (Scope : X 100)

Matrix Table of Solder Joint Test

Type	Chip Area	CTE	Remark
A	120.7 mm^2	5.96 ppm/℃	T/C condition : -65 ~ 150℃
B	61.8 mm^2	10.3 ppm/℃	
C	61.8 mm^2	10.3 ppm/℃	Adding anchor leads at short body

. Package size : 10 x 16 mm^2

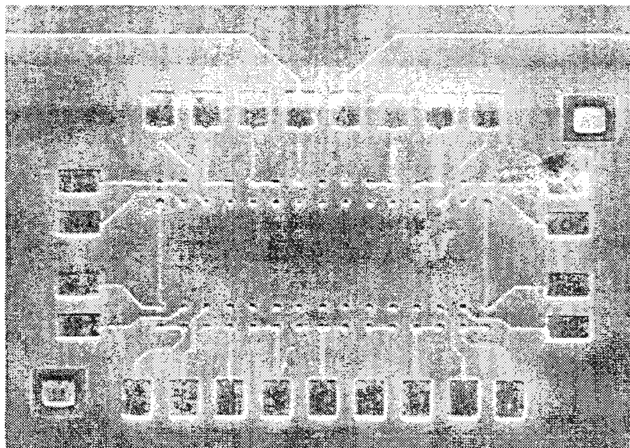
. CTE of PCB : 15 ppm/℃

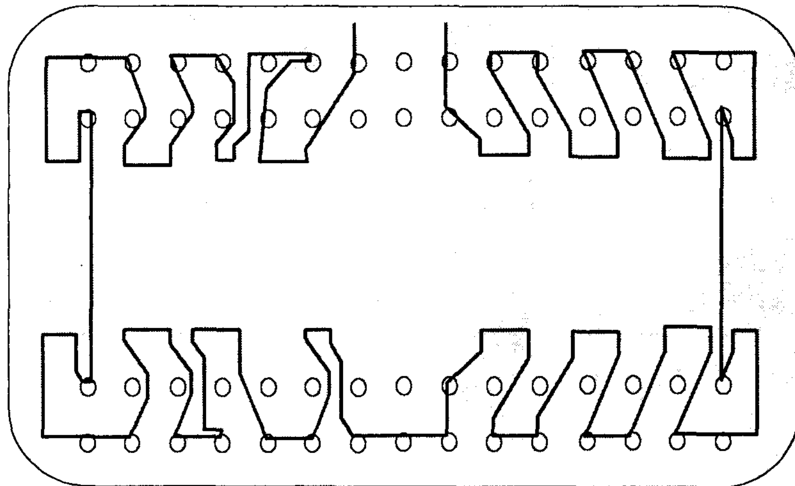
. Daisy Chain Board : NSMD Type, Ni/Au Electroplated

Daisy Chain Structure

. Connected series circuit for outer balls at daisy chain board

. Connected inner leads in the package





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Solder Joint Reliability

Weibull Cumulative

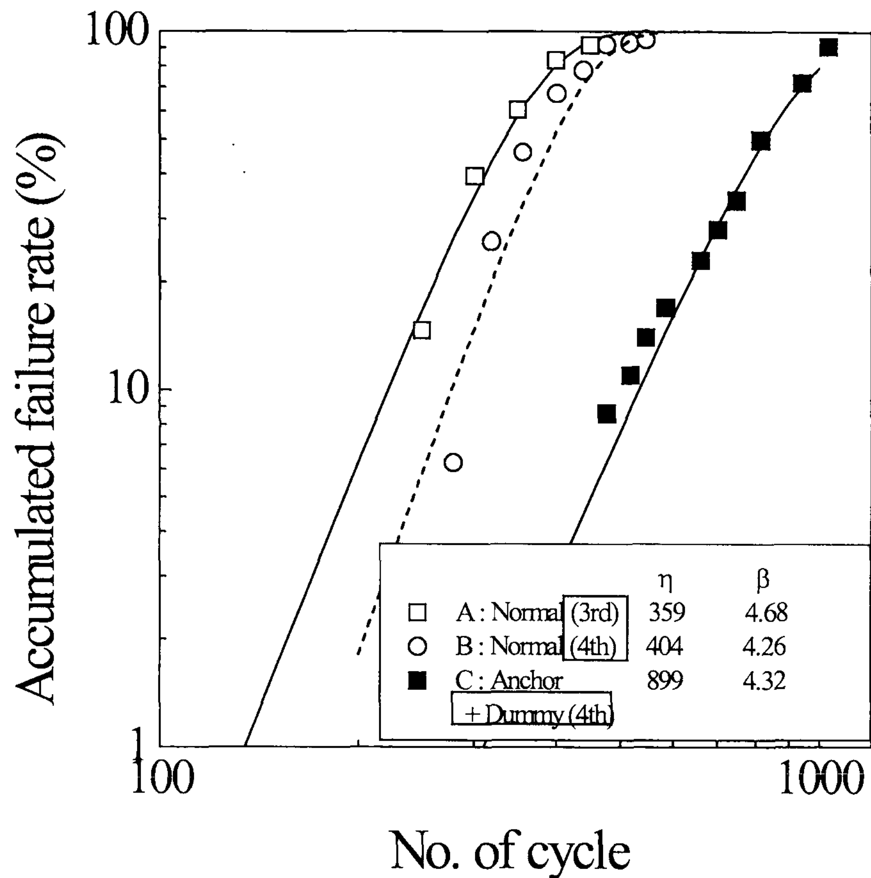
Distribution Function

$$F(t) = 1 - \exp\left(-\frac{t}{\eta}\right)^{\beta}$$

Where is t : Time to cycle

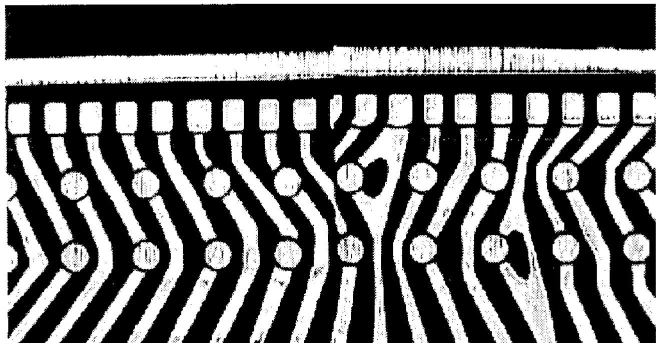
η : Characteristic life

β : Shape parameter



Capacitance of Lead Frame Shape

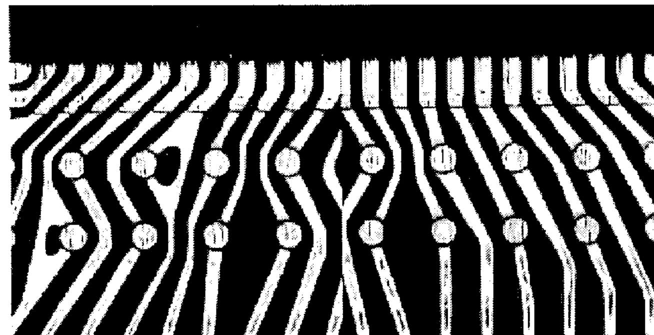
< Type A>



Not uniform at right side

(Input pins)

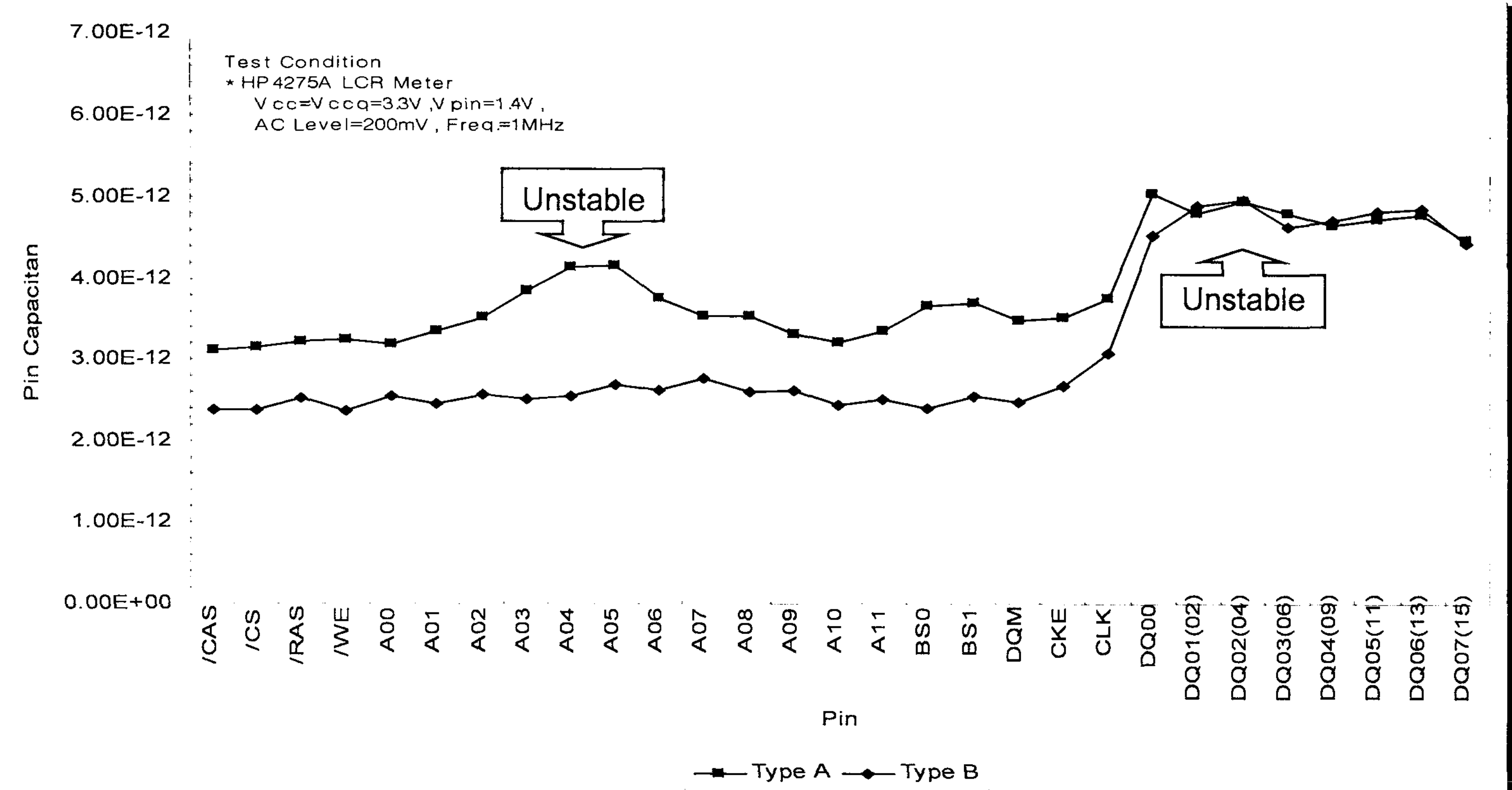
<Type B>



Not uniform at left side

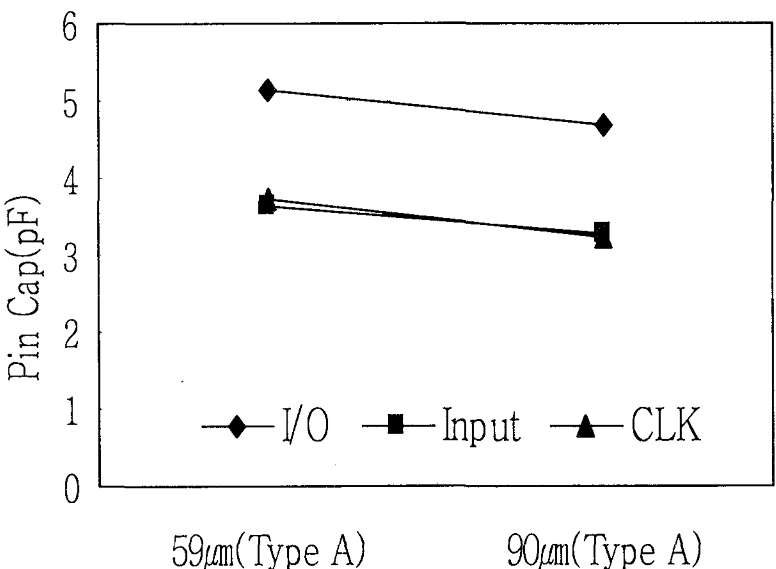
(I/O pins)

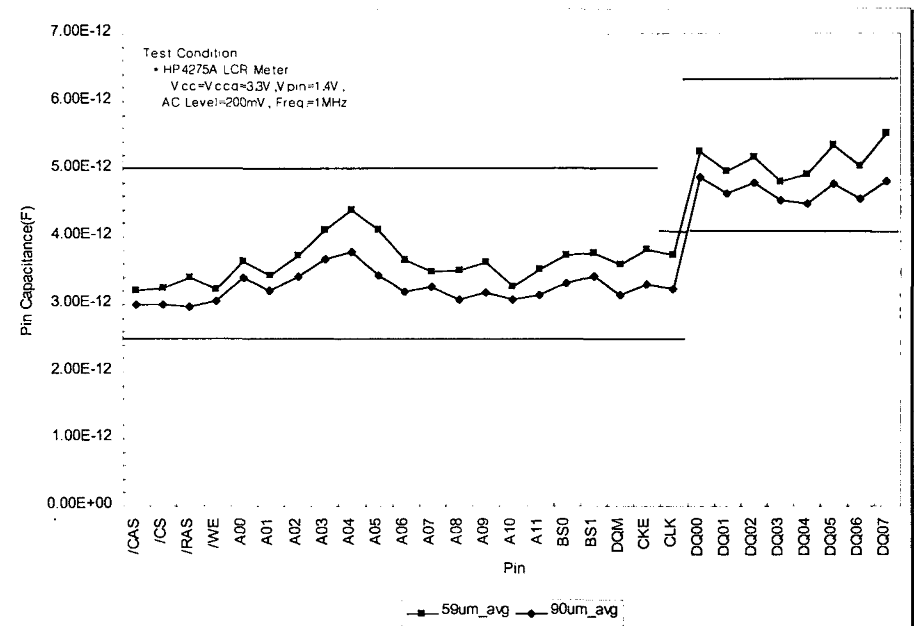
Capacitance Measurement



☞ Uniform Inner Lead shape has stable capacitance.

Capacitance Depend on Tape Thickness





☞ As tape thickness has thicker, the capacitance has lower values.

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Comparison Relative Cost for Packages

Package	Material Cost	Total Assembly Cost
TSOP	47	100
LF-CSP	75	130
FBGA	150	200
uBGA	200	300

Summary

- New CSP using Lead Frame and solder ball techniques.
- EMC needs high filler content, low CTE and high flexural modulus.
- Solder Joint Reliability improved by anchor leads.
- Uniform inner lead shape would be better at capacitance values.
- Low Assembly cost CSP.