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Outline

Needs of Area Array Package

Market Review of BGA, CSP and Flip Chip

Hot Issues and iKey Technologies

- BGA
- CSP
- Flip Chip

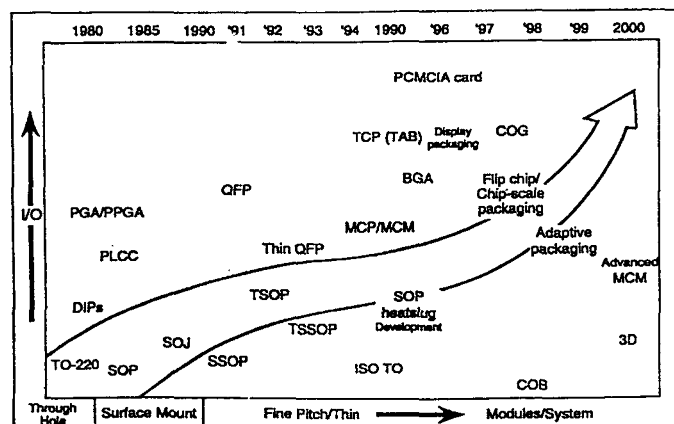
Conclusions

Trends of Packaging Technologies

Driving Forces

- Miniaturization ; smaller, thinner, lighter
- Performance ; better electrical and thermal properties
- Cost ; cheaper, outsourcing

Package Roadmap



Why do we need area array packages ~

Progress of IC technologies

high I/O pins due to reduced feature size, high integration

more and more transistors on chip, bigger and bigger chip size

higher I/O pins more than 400 pins

high speed ICs and increased SSO ($\Delta I = n L \ di/dt$)

clock frequency exceeding 300 MHz

high bandwidth above 3 GHz in RF applications

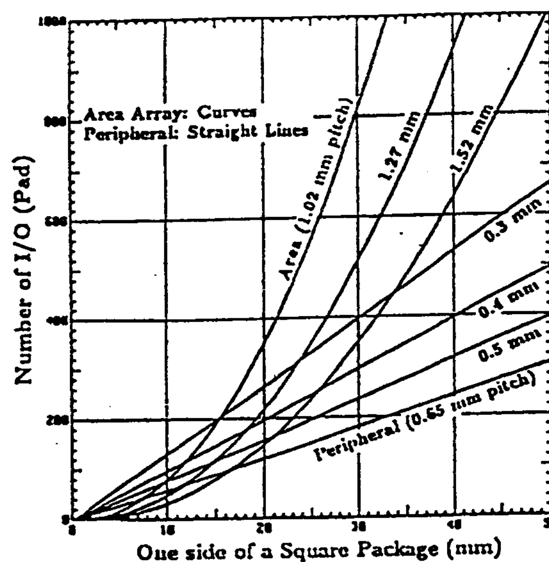
as a rule of thumb, power/ground pins requires 30 ~ 40 % of total pins

low inductance, short interconnect

beyond the capacity of plastic packages with peripheral leads

Why do we need area array packages ~ (continued)

Miniaturization



peripheral leads -> area array leads

Why do we need area array packages ? (continued)

Electrical Performance

	PBGA			PQFP		
Leads	*169*	*225*	*324*	*132*	*208*	*304*
L (nH)	3 ~ 8	3.7 ~ 11.9	4.3 ~ 11.4	3.8 ~ 5.3	5.4 ~ 7.1	9.4 ~ 11.6
C (pF)	0.7 ~ 1.8	0.7 ~ 1.8	0.9 ~ 2.2	0.7 ~ 1.0	1.2 ~ 1.5	2.0 ~ 2.2

easy to assign GND/PWR pins to minimize the their inductance

as to inductance, BGA > fine pitch BGA > CSP >> flip chip

Historical Perspective of Area Array Package

1964 - IBM first introduces C4 Flip Chip

1978 - Pin Grid Array Introduced

1984 - Motorola uses Ceramic Land Grid Arrays

1986 - Motorola replaces ceramic with BT,
develop overmolding process with Citizen

1989 - Motorola starts using OMPAC in products

1992 - Compaq uses PBGAs in PCs.

Mid-1990's - many CSPs introduced
- μ-BGA of Tessera is the most common CSP

Market Overview

BGA

over a billion by the end of 1999

continue to grow

flip chip-BGA, fine pitch BGA

CSP

exceed two billions by the 2000

not just an interim package

SRAM -> RDRAM -> Non-memory(ASIC, DSP, etc)

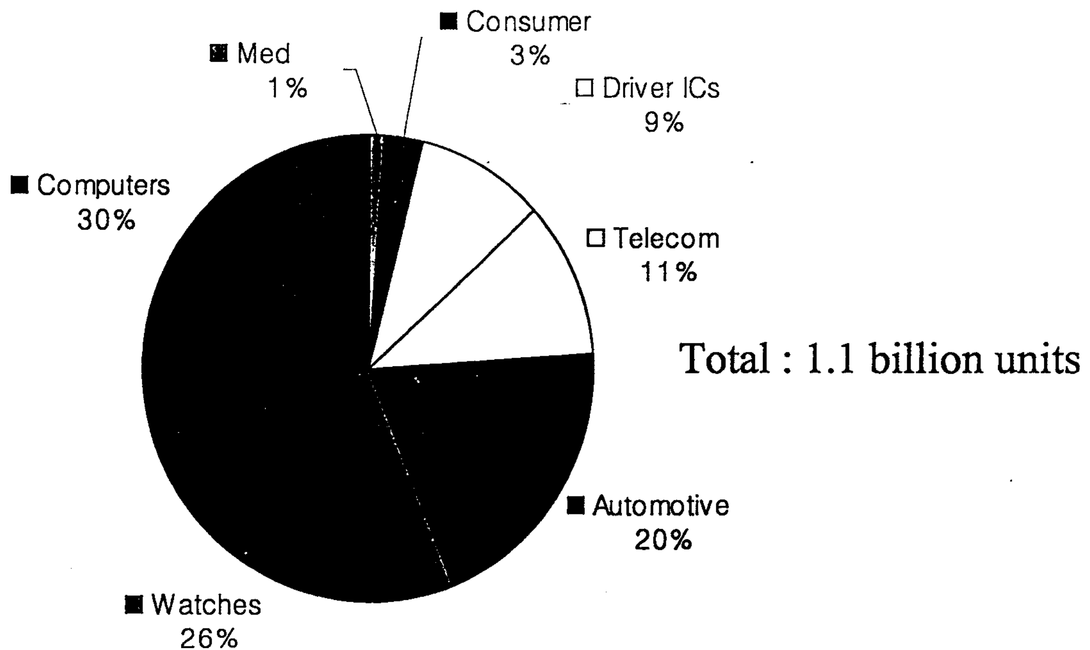
hot new developments at wafer level-CSP

Flip Chip

400 ~ 600 millions for 1998, over a billion in 2000

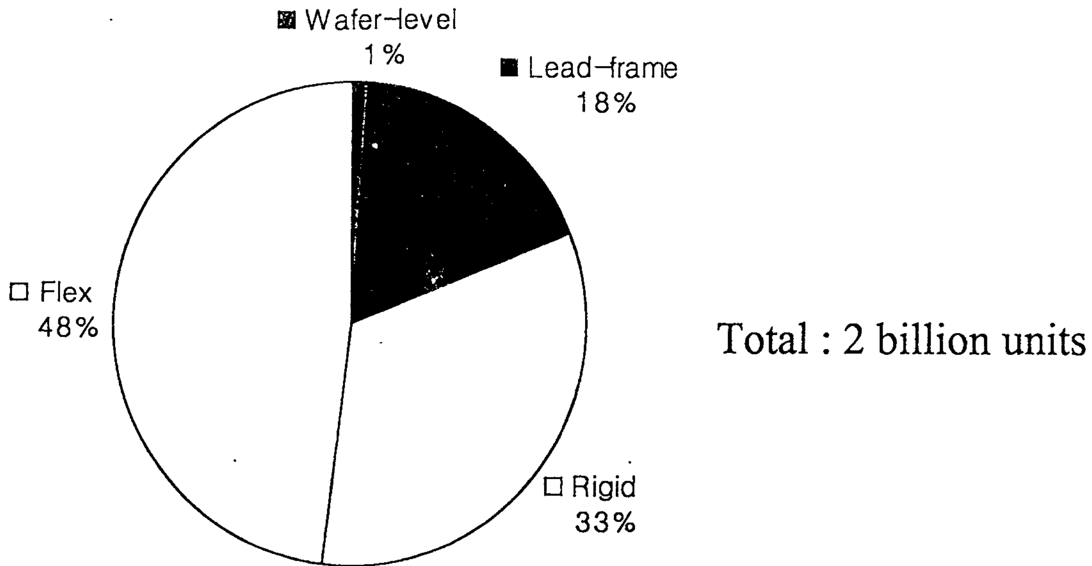
growth is primarily inside package

Year 2000 Flip Chip Mounting



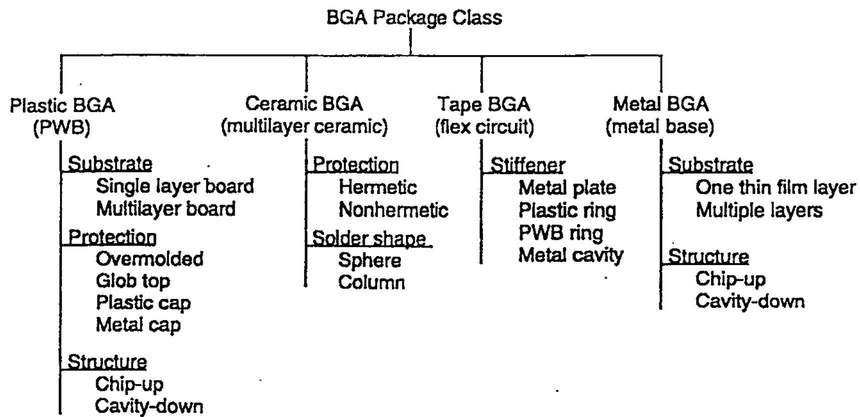
Source : Advancing Microelectronics,1999

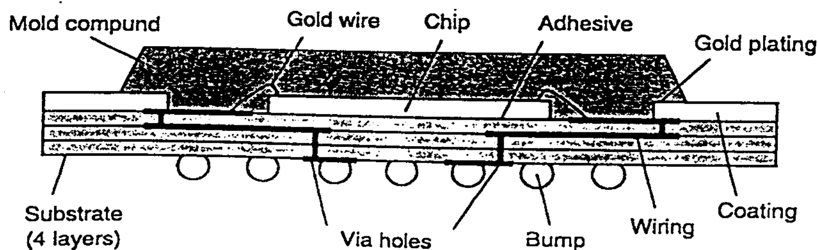
Year 2000 CSP Shipments



Source : Advancing Microelectronics,1999

BGA Package





Advantage and Weakness of PBGA Package

Advantages

- high I/O, improved electrical & thermal performances
- multichip capable
- moderately low height profile
- smaller CTE mismatch with PWB
- compatible with existing SMT
- coarse pitch & self-aligning -> high assembly yield
- low susceptibility to lead damage
- migration path to CSP and flip chip processing

Weaknesses

- solder joint inspection requires X-ray; not easy to inspect
- moisture sensitivity of thin molded packages (corrosin, popcorn, etc)
- local CTE mismatch strongly affected by die size -> warpage
- not good to rework
- cost, especially at low pin counts
- high I/o usually demands multilayer PCBs
- lack of dimensional control

Solder Balls

Standard alloys

- SnPb eutectic(63/37, 183 °C) ; PBGA, some CBGA
- High Pb(10/90, 302 °C) ; CBGA, TBGA, some PBGA
- SnPbAg(62/36/2, 179 °C) ; PBGA, some CBGA

Fatigue resistant alloys

- InPb (19/81), InSn (52/48)

Lead free alloys

- In, Ge based

Solder Ball Defects

- solder bridging, missing ball
- solder voiding due to excessive flux or insufficient mixing of paste
- require the X-ray inspection after assembly

Fine Pitch BGA Packages

Major categories of Fine Pitch BGA Packages
- Fine Pitch BGA (FBGA)
  - a reduced-pitch version, < 1.0 mm, of a BGA
  - in addition, total profile height is 2.0 mm
- Low-Profile Fine-Pitch BAG (LFBGA)
  - a reduced-height version, 1.7 mm, of a FBGA
- Thin-Profile Fine-Pitch BGA (TFBGA)
  - a reduced-height version, 1.2 mm, of a FBGA

Technical Issues
- low profile, short wire length wire bond
- reliability ; popcorn crack, corrosion,
- fine pattern PCB ; SLC
- encapsulation : molding defects such as incomplete mold, excessive warpage
- assembly yield

Applications
- a cost-effective BGA compatible with CSP
- memory ICs with high speed and high pin

BGA Rework Process

Identifying the defects and its cause by X-ray inspection

Removing the failed component by local heating

Cleaning the site and reballing the BGA

Re-applying solder paste to land pad

Replace BGA on PCB

Re-attaching

Inspection

Technical Issues in PBGA

Substrate

fine patterned line/space ; less than 4 mil/4 mil (SLC)
layout design, to minimize signal noise such as SSN, crosstalk
optimized solder pad design ; land size, soldermask opening

Packaging process

die attach, wire bond and mold process for fine pitch BGA, smaller BGA
warpage control after molding, which is sensitive to die size, package structure
flip chip BGA
PBGA compatible with the pitch of CSP, especially high pin I/Os

Reliability

not good reliability due to moisture sensitivity ; popcorn crack, corrosion,
solder joint reliability, especially in thin PBGA

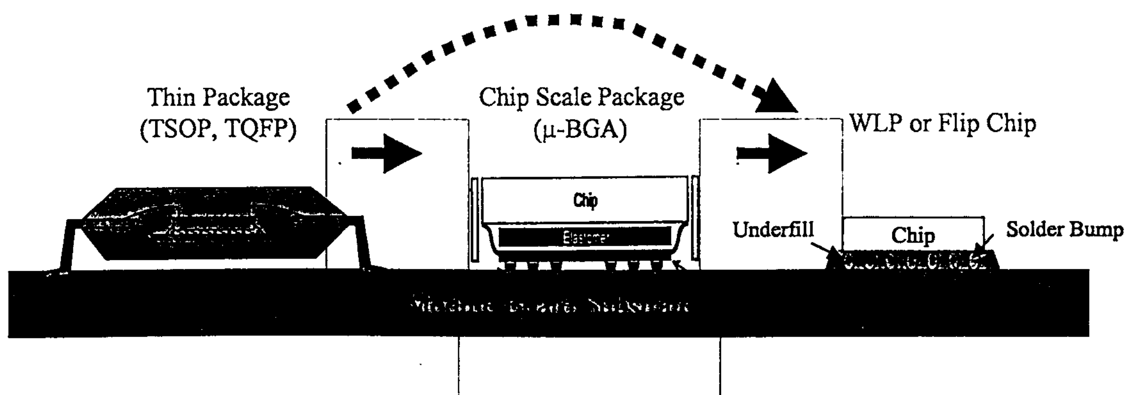
Cost Reduction

more expensive than plastic package, still now
less packaging yield
need to develop cheaper materials such as die adhesive, EMC, PCB

Assembly

insufficient experience to assemble high pin BGA on mother board
rework process

Package Trend for High Speed Memory ICs



peripheral -> area array

∴ plastic package -> fine pitch BGA/CSP -> WLP or Flip Chip

high speed memory IC will require high I/O and better electrical performance

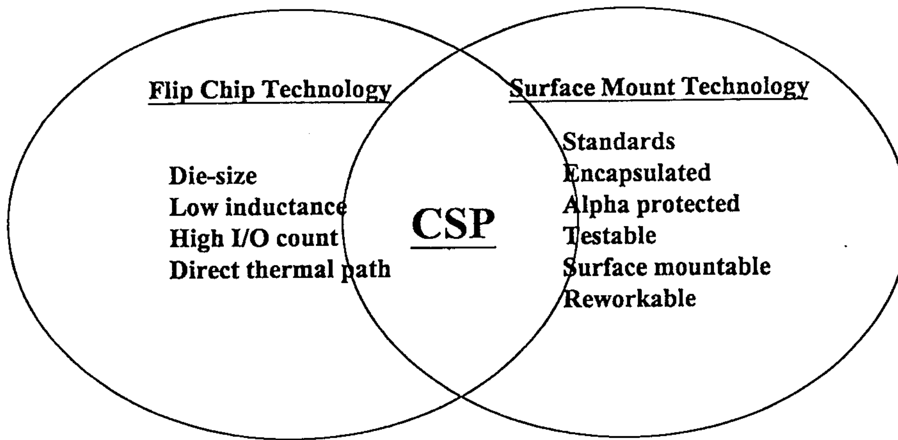
WLP(wafer level packaging) may be a big hot issue in memory semiconductor makers

CSP(chip scale package)

Features

- package foot print is less than 120 % of chip area
- easy to test at speed, burn-in for KGD, assemble, standardize, rework, etc

Background

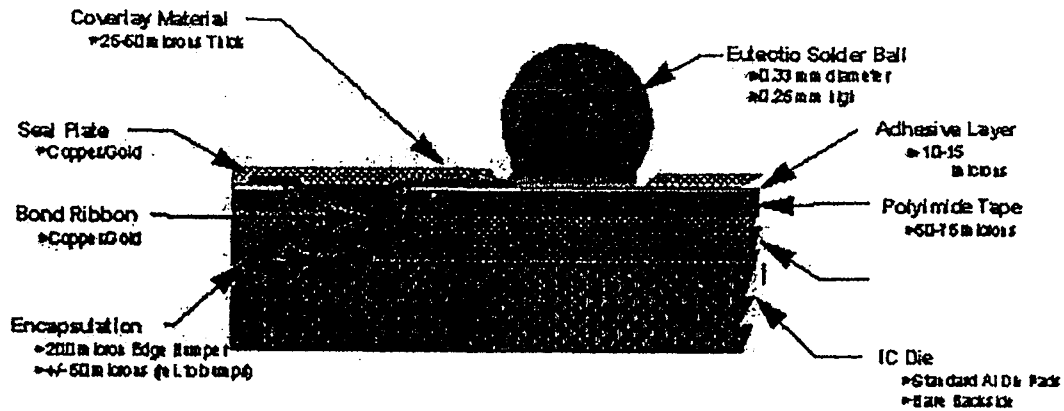


Typical Types of Worldwide CSP

Flex Circuit Interposers	Rigid Substrate Interposers	Custom Lead Frames
General Electric	IBM	Fujitsu
NEC	Matsushita	Hitachi Cable
Nitto Denko	Motorola	Hitachi Cable
Tessera	Toshiba	LG Semicon

Wafer-Level Assembly	Molded Package	TCP Lead Frame
ChipScale	Mitsubishi	Rohm
ShellCase		

μ-BGA Package Structure (Tessera)

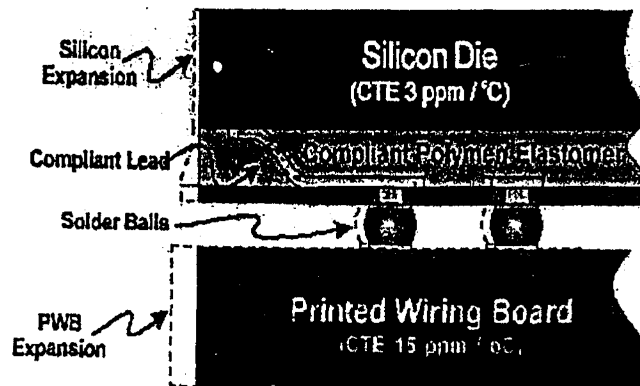


Applications

- SRAM, Flash Memory
- DRAM, Rambus DRAM
- Logic devices for potable products

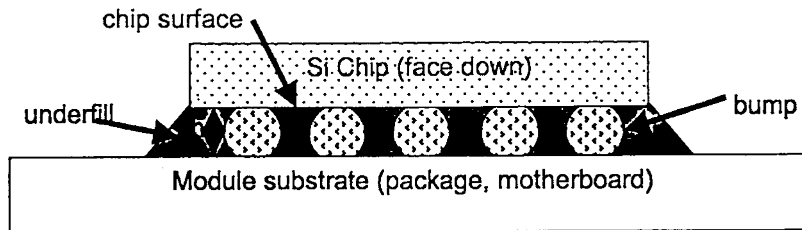
Technical Issues of μ-BGA

- Au coated Cu beam tape
- not matured technologies in materials and equipments
- relatively high cost -> need cost reduction
- not perfect solution for high pin package
- beam lead and solder joint reliability in large dies



Flip Chip Technology

Vertical view



flip chip
- in - package
  - driven by IC makers such as Intel, National, LSI Logic, AMD, etc
  - increasing market
- on-board
  - driven by system providers such as IBM, HP, Lucent, Delco, etc
  - difficult to estimate due to being deeply embedded in system
  - until now, main portion of flip chip market

Flip Chip Technology

	Advantages	Disadvantages
1. Performance	- low inductance - short interconnect length - low thermal resistance	- insufficient electrical data - need to study CWP lines
2. Manufacturing	- no thinning, no back metallization - high yield - low cost	- immature process - required bump process
3. Assembly	- reduced size and weight - self-alignment during solder reflow - SMT compatibility	- requires underfill sometimes

Technical Trends of Flip Chip Technology

	Past	Present	Future
UBM	- Cr, Ni	- Ti, TiN, TiW	-
Bump process	- evaporation - 97Pb3Sn	- electroplating - eutectic solder - 95Pb5Sn	- electroless - stencil printing - leadless solder
Bump Pitch(Mass.)	- 300 ~ 350 um	- 200 um	- < 150 um
Substrate	- multilayer ceramic	- fine pattern PCB - fine pattern tape	- thin film substrate
Applications	- computer, military ,MCM	- PC, telecom., consumer IC, MMIC	- wide applications

Key technologies in Flip Chip

UBM

sputtering ; Ti, Ni, Cr, Cu, Au
electroless plating ; Ni/Au

Bump formation

how to reduce bump cost
evaporation ; 19%
electro/electroless plating or stencil bumping ; 78 %
stud bump ; 3 %

Flux

flux type ; no clean flux, water clean flux
process to clean residues after reflow

Redistribution

Cu/BCB process for peripheral pad -> area array pad
how to stress release

Key technologies in Flip Chip (continued)

Substrate
- ceramic, FR-4, BT-resin, Flexible circuit
- fine pattern and small via
  - line and space ; down to 50 um, via diameter ; < 100 um
- multi-layer build-up PCB

Underfill
- properties characterization of underfill materials
- to obtain both productivity and reliability

Solder joint reliability
- structure effects ; pad structure, bump material and bump dimension, chip size
- material effects ; chip size, substrate material, underfill
- to improve the thermal cycling fatigue life-time

RF Applications of Flip Chip

Company	Function	Technology	*freq.*	Features
Hughes 97	- Driver Amp. - VCO - Static Fre. Divider	- SiGe - Bipolar	Ku-band	- Polyimide microstrip MMICs ; Top layer : ground plane ; Si-based devices
	- MIC Amp - Fre. Divider	- InP based HEMT	Ku-band	- Flip-chip MICs ; solder bump
NEC 98	- LNA	- CPW MMIC - GaAs	- 30 GHz - 60 GHz	- Co-planar waveguide line - Bare chip thick : 150 um - 20 um high Au bump : Thermal compression - with or without underfill - Flip Chip on Al2O3 substrate ; Performance Test, S-Parameter
Fujitsu 98	- Automotive Radars chipset	- 0.15 um InGaP/ InGaAs HEMT	- 76 GHz	- chipset consisting of 76GHz Amp, mixer, SPDT switches, 38/76GHz doubler, 38GHz VCO, and 38GHz buffer amp. - Co-planar waveguide MMIC - Co-planar waveguide Al2O3 substrate (Sn pad) - 20 um high Au bump, d=40 um
NEC 98	- 3 stage Amp.	- GaAs	- W-band - 77 GHz	- Co-planar waveguide line - Bare chip thick : 150 um without metal - 20 um high Au bump : Thermal compression - with or without underfill - Flip Chip on Al2O3 substrate(CPW)

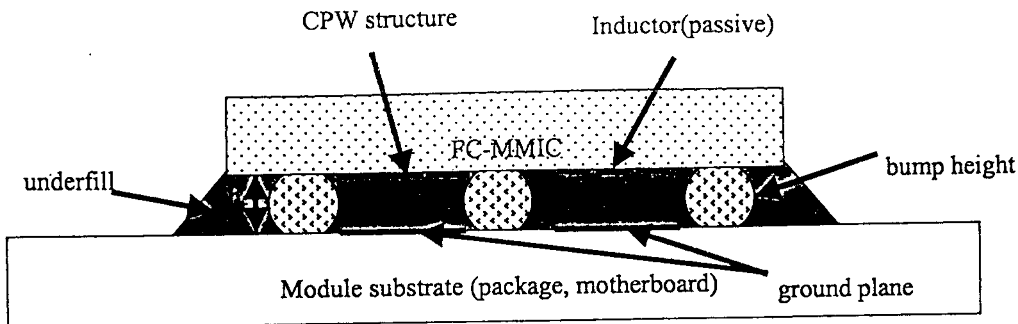
RF Applications of Flip Chip

Company	Function	Technology	freq.	Features
Fraunhofer Institute 97	- CPW line	- GaAs	- 10 ~ 120 GHz	-Difference of Electrical results between CPW line of Flip chip and CBCPW(conductor backing)
GM Huges 95	- T/R Module	- CWP based circuitry - MESFET		- Ag plated bumps for electrical interconnect ; 75 um ~ 90 um high - T- shaped thermal bump
Univ. of Colorado at Boulder 98	- Characterization on CWP line and its RF performance	- GaAs - 50 Ω CWP line		- Solder joint reliability and performance degradation with or without underfill ; d=150 um, h=70um, die thick=635um - GaAs on ceramic or Duroid substrate - Ag-bump for RF Performance ; h=75 um, d=150 m, - Au(5um)/Ti(0.02um)/ceramic - Additional degradation due to underfill was less than 1dB
Sharp 98	- GSM class V PA	- AlGaAs/GaAs HBT	-900 MHz	- FCB on Al2O3 - Low profile package (6.35X6.35X1.05 mm3)
Univ. of Massachusetts	- Modeling			- Both coplanar and microstrip chips are circuit modeled and their results are compared.
Univ. of Michigan	- Low noise Amp.	- Inp HEMP	- K-band ; 20 GHz	- Si micromachined conformal package

RF Applications of Flip Chip

Company	Function	Technology	freq.	Features
Fujitsu 98	- 2 stage Amp.	- 0.15 um InGaP/ InGaAs HEMT	- W-band (79 GHz)	- Co-planar waveguide MMIC ; 600 um thick, 2 um thick Au line - Co-planar waveguide Al2O3 substrate (Sn pad) - 20 um high Au bump, d=40 um (Au/AuSn) - Z_0 measurements of transmission line (EM anal.)
Huges	- HPA	- 0.25 um PHEMT	- X-Band	- Bump : Ag plating, h=100 um, d= 150 um - 40 % enhanced thermal performance - 40 % reduced cost
GEC Caswell 98	- PA, VCO - for HIPERLAN	- GaAs MMIC - Via provessing - Flip Chip on MCM-D	- 5.2 GHz	- At FCB, GND plane must be removed under Inductor of FC-MMIC - Solder bump - MCM assembled with 17 mm BGA
Siemens 98	- CPW line - Filters - PA	- Poly Diamond Substrate - GaAs MMIC PHEMT	- 1 ~ 120 GHz - 28 GHz	- PE-CVD processing Diamond wafer ; tanδ as low as $4X10^{-5}$, ε_r = 5.7 0.05 at 145 GHz - Electrical characterization of CPW - Flip chip on diamond - Au bump without back thinning
Raytheon 98	- ETL Amp.	- GaAs MMIC - BeO μ-BGA	- 10 GHz	- not thinned (635um) - 25 um PI, RF GND plane(top) - 10 mil solder ball BeO μ-BGA
Raytheon 98	- ETL Amp.	- GaAs MMIC - pHEMT - BeO μ-BGA	- 11.5 GHz	- not thinned (635um) - 25 um PI, RF GND plane(top) shielding - Z-axis chip adhesive interconnect - 10 mil solder ball BeO μ-BGA

Key Technologies in RF Flip Chip



- CPW structure : width/space of GSG, line thickness, linemat'l
- effect of structural factors on the performance of CPW or inductor(or other passive)
  - ground plane, substrate mat'l, bump height, underfill, backside metallization
- comparison of electrical performance between FC-MMIC and wirebonding-MMIC
- thermal resistance
- T/C reliability

Conclusions

BGA

CBGA, MBGA , TBGA ; more than 500 pins
PBGA ; 250 ~ 500 pins
flip chip BGA will be increasingly developed for high speed ICs.
big concerns about Fine-Pitch BGA or Smaller BGA
migration path to CSP and flip chip processing

Flip Chip

the market of flip chip in package such as Flip-PBGA will gradually increase
a wafer level-CSP using flip chip technology is a hot issue
In spite of many merits, there are still existing obstacles
such as bump cost, test, infrastructure, etc

CSP

suitable for low power(<1W) ICs, memories, and ASIC(< 200 pins)
not just an interim package
application of CSP will be broadened ; SRAM -> RDRAM -> ASIC, DSP, etc