Development of a new wafer level package by using a redistribution technique

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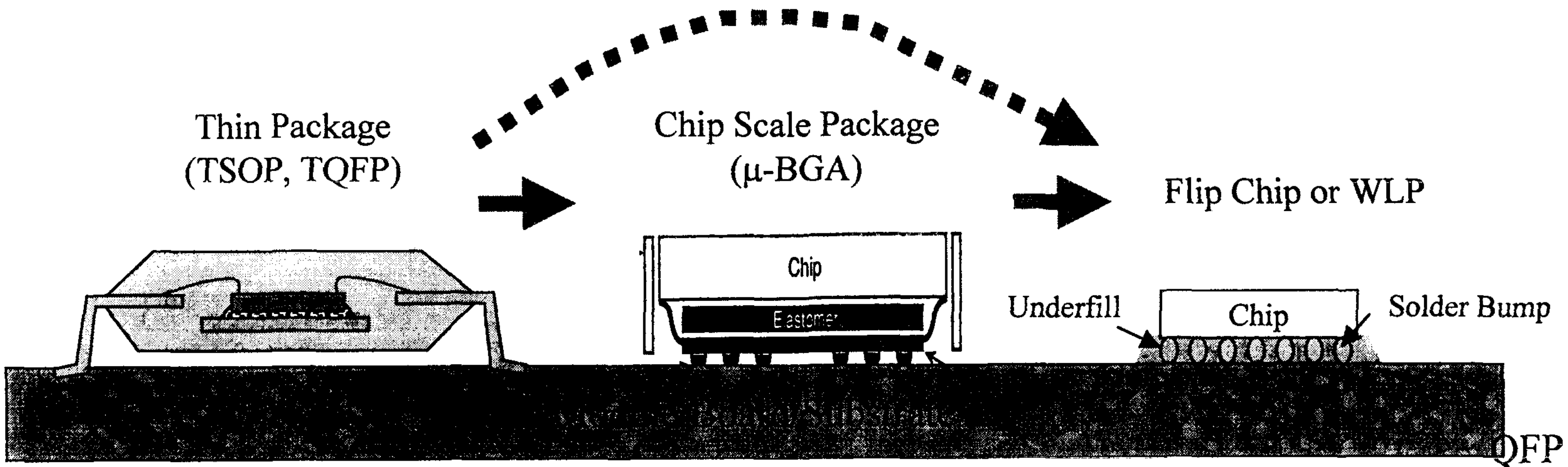
Recent Package Technologies



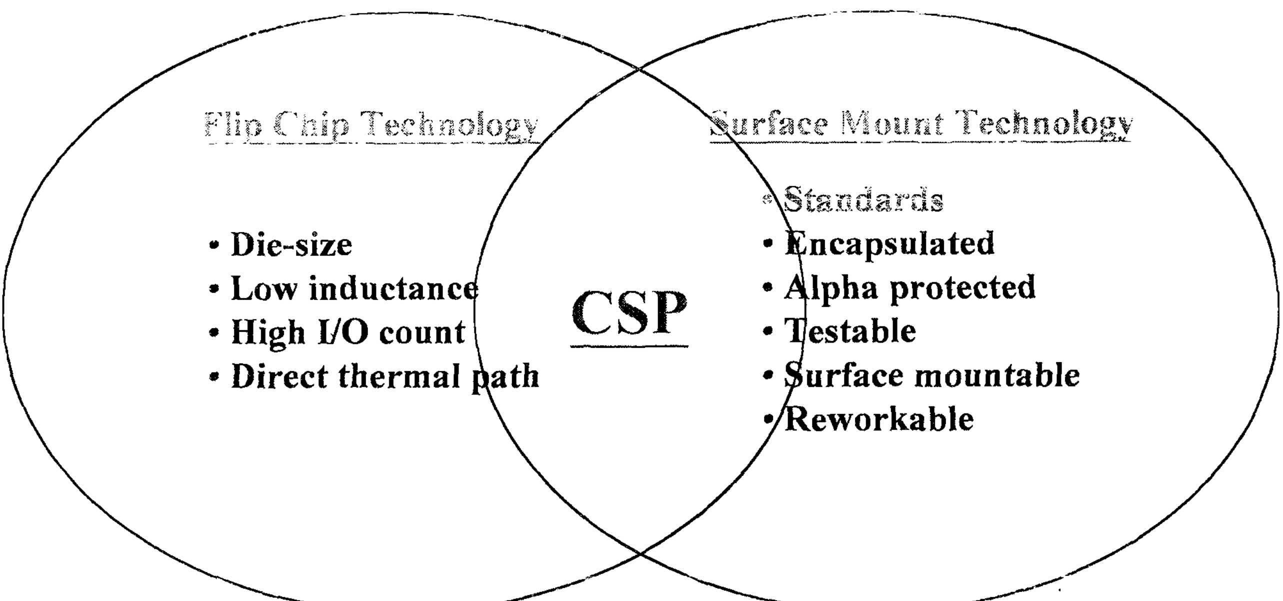
- Driving Forces
  - Miniaturization ; smaller, thinner, lighter
  - Performance ; better electrical and thermal properties
  - Cost ; cheaper, outsourcing

BGA

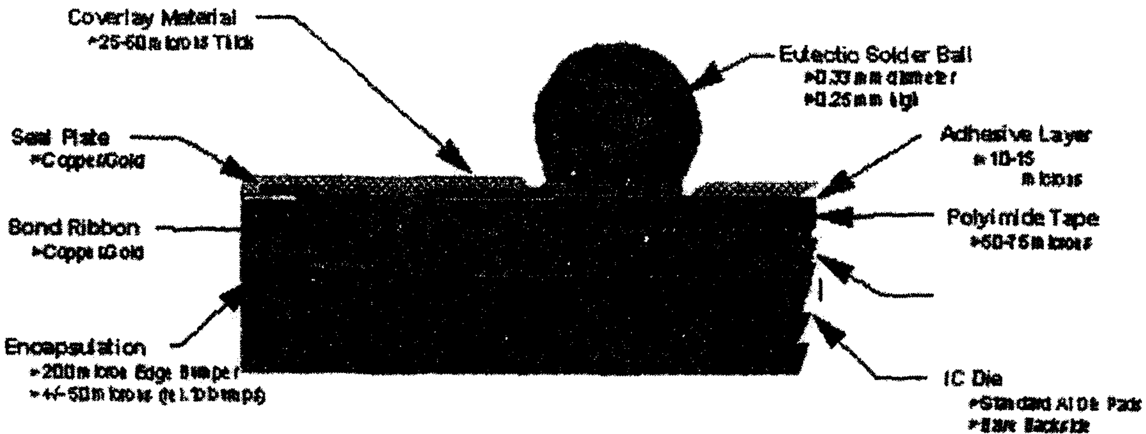
Chip Scale Package ?

- Features
  - package foot print is less than 120 % of chip area
  - 0.8, 0.75, 0.6 mm solder ball pitch
  - easy to test at speed, burn-in for KGD, assemble, standardize, rework, etc

- Background



Trends of CSP



- Issues of μ-BGA
  - Au coated Cu beam tape
  - not matured technologies in materials and equipments
  - relatively high cost -> need cost reduction
  - not perfect solution for high pin package
  - beam lead and solder joint reliability in large dies
- Recent Trends
  - Lower Cost, Higher Reliability
  - Fine Pitch BGA, WB-CSP

What and Why WLP ?

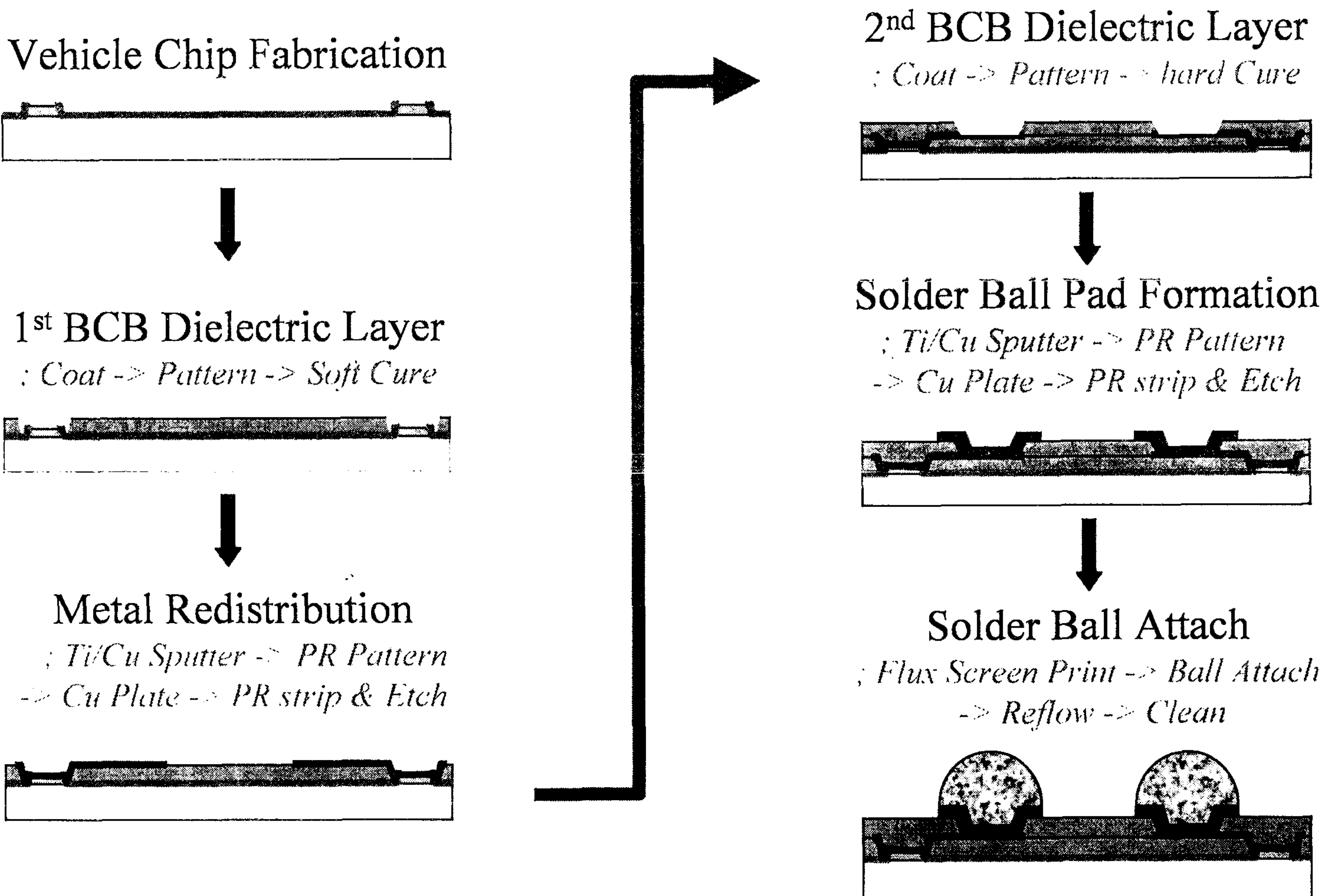
- Definition
  - WLP packages ICs while they are still in wafer form instead of chip form
  - WLP typically replaces die bond, wire bond, and encapsulation by wafer processes such as photolithography, metal deposition, dielectric deposition, etc.

- Features
  - Lower cost due to wafer-level batch process
  - Miniaturization : True chip size
  - Matured process technologies
  - Performance : short length and controlled dimensions
  - In particular, more suitable for memory devices ($\leq$ 150 pins)
  - Migration path to flip chip

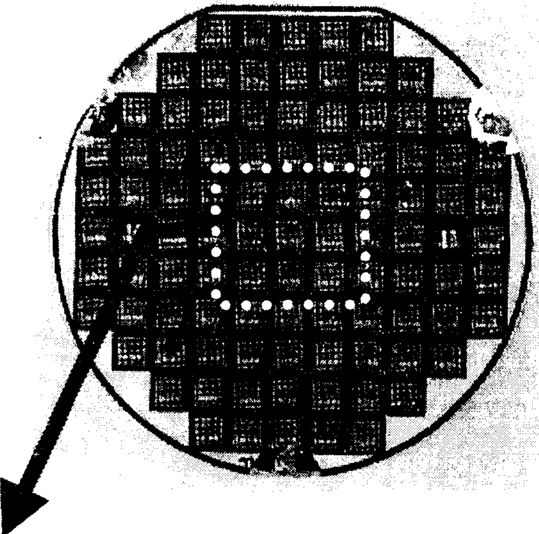
Types of WLP-CSP

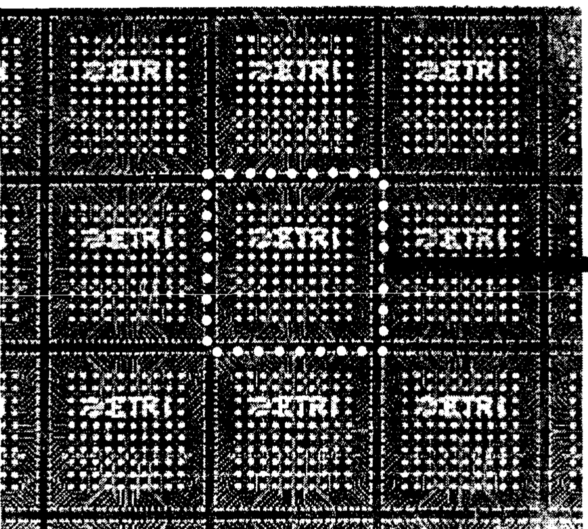
- On-Wafer/Chip Redistribution (OWRD)
  - Simple process
  - Concern of solder joint reliability
  - Key players : Aptos/Sandia, FCT, Toshiba, Hitachi, National, etc.
- On-Wafer/Chip Redistribution with Encapsulation (RDWE)
  - Similar to OWRD
  - Non-standard wafer process
  - Key players : Fujitsu, Casio/Oki, Mitsubishi, etc.
- On-Substrate Redistribution (OSRD)
  - Similar to conventional CSPs
  - Concern of cost
  - Key players : Amkor (W/B-WLP), NEC, Tessera, etc.
- Wrap-Around & Redistribution (WARD)
  - Complicated processes, Suitable for peripheral I/P
  - Key players : ShellCase, ChipScale, Intarsia, etc.

Process Procedures of WLP-CSP



Example of WLP-CSP





Summary

- New WLPs of 750 μm solder ball pitch have been developed by using a Cu/BCB multilayer process.

- The BCB1/UBM interface was found to be the weakest interface in the WLP.

- With Ar+ RF treatment on BCB surface, we could achieve the sufficient solder ball shear strength.
  - – Shear Strength : 9.8 MPa -> 38.1 MPa

- The crack was propagated to the interface between Cu and Ti above BCB1.

- The solder joint reliability will be studied.

ETRI