40 Years of Advances in the Silicon Wafer Industry and the Evolution of an Engineered Wafer

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Introduction:

Two major breakthroughs in the late 1950s laid the foundation for the birth of what has become one of the fastest growing and rapidly evolving industries in the world today. One was the integrated circuit (IC), invented by Jack Kilby of Texas Instruments in 1958 [1]. It provided a major breakthrough for semiconductors, demanding yet better quality and larger quantities. The other was Dash's necking process [2], which allowed growth of dislocation-free silicon crystals. It also facilitates the growth of larger diameter crystals, at higher crystal growth rates compared to dislocated crystals.

Interestingly, both the first transistor and the first IC were first fabricated on a substrate of germanium. Despite its scarcity, germanium initially proved to be easier to purify and work with, both in a laboratory environment and on production lines. It was only in the latter half of the 1950s that the industry moved on to the much more abundant silicon. Perfection of float-zone refining and other silicon purification techniques during the mid-1950s allowed silicon to finally pull abreast of germanium [3]. The main advantages of silicon over germanium are its larger band gap and the ability to readily grow and sustain a protective oxide layer.

Great strides have been made over the last 40 years in understanding defect formation and their effects on device performance. The advent of dislocation free silicon crystals revealed the presence of striated patterns, which were classified as A- and B-defects [4]. Later another class of intrinsic point defects, called D-defects, which were agglomerated vacancy-type defects were identified [5]. Carbon was thought to play a role in the formation of A and B-defects. It had also been identified as a contaminant and a source of device failure from the early float-zone days [6,7]. Advances in the understanding carbon incorporation routes into the crystal and controlling them resulted in lowering carbon levels to close to detection limits (0.05ppma) [8]. Oxygen became an important impurity with the transition from float-zone to Czochralski silicon. Its role in silicon changed with the discovery of its gettering properties, from being a harmful impurity, to one that is critical for high device yields [9].

Understanding the behavior of intrinsic point defects, and their effects on defect formation and oxygen precipitation have furthered our knowledge enormously. This has resulted in the engineering of wafers, with controlled type and concentration of intrinsic point defects and also an optimal level of oxygen precipitates to meet each device manufacturers' unique requirements [10]. By employing these techniques in certain ways,

silicon wafers can be effectively programmed to produce a defect free surface region, with metal gettering properties in the bulk.

The Semiconductor Industry Today:

Before we examine the technical advances in silicon over the last 40 years, it is beneficial to look at the current state of the semiconductor industry and the impact it has had on the world.

Intel founder Gordon Moore's early observation that semiconductor component density (components per unit area) will double every 18 months is probably one of the most quoted relationships in the semiconductor industry. True to his predictions, the IC industry has grown at a phenomenal rate of 25-30% (compound annual grow rate) [11]. In the past 10 years, the semiconductor industry has expanded dramatically from $30 billion to $150 billion and is expected to grow to $300 billion by the year 2000.

Semiconductor content of electronic equipment has been growing at an even faster pace. Semiconductor content in PCs was about 30% in 1995 and is expected to increase to about 40% by the end of this year. Semiconductor content of all electronic equipment has increased from about 10% in 1990 to about 20% today, and continues to increase. This is clear indication that semiconductors are driving growth in the electronics industry. They propelled it ahead of the automotive industry, to become the world's largest industry, in 1996 [12]. The silicon wafer industry, the subject of this paper, is at the bottom of this industry pyramid and forms the foundation of the electronics industry. In 1998, its size was estimated to be about $5 billion.

Technical Advances in Silicon:

Silicon Single Crystal Growth:

Four factors have contributed to the semiconductor industry's ability to stay on the enhanced productivity learning curve predicted by Gordon Moore. They are (a) shrinking lithographic design; (b) yield improvements; (c) increased equipment utilization; and (d) larger wafer diameters [13]. Of these, increasing wafer diameters has been the key to helping the industry achieve the required economy of scale for large volume IC manufacturing.

Until 1959, the specifications for discrete devices drove the requirements for single crystal diameters from 38 to 51mm. This evolution was slow, when compared to transition from 51mm to 200mm diameter crystals that occurred in the following 30 years. Today, the industry standard crystal diameter is 200mm and conversion to 300mm diameter crystals has begun [14].

Crystal growth method and the size of equipment used to grow these large crystals have rapidly evolved over the last 30 years. Siemens was the pioneer in the development of processes for synthesis, purification and crystallization of semiconductor silicon [15]. In

the early 1960s, Siemens used a vacuum ambient in its Float-Zone (FZ) process to grow silicon crystals that contained dislocations. The following ten years saw enormous advances in the ability of the FZ process to grow dislocation free crystals with controlled doping and reduced impurity levels. Annual production of FZ monocrystalline silicon also ramped from 22kg to 14 tons between 1959 to 1969 [15].

Inherent limitations of the FZ process were recognized early by researchers at Bell Laboratories and General Electric. In 1950, Gordon Teal and John Little [16] applied the Czochralski (CZ) crystal pulling process, with some modifications, to grow single crystals of germanium (19mm diameter). Teal and Buehler [17] later demonstrated the growth of single crystal silicon of comparable size and chemical purity using the CZ method in 1952.

Czochralski's method is technologically superior and less costly than the FZ method and facilitates the growth of single crystals of any size and shape. Today, about 90% of the world's silicon single crystals are produced using the CZ method, with the remaining 10% produced by the FZ method.

The increasing diameter of silicon crystals has resulted in CZ crystal pullers that are close to 30ft tall for 400mm diameter crystals, compared to about 14ft tall pullers for 150mm diameter crystals. Initial weight of silicon charged into a crucible and the crucible diameters needed to grow the larger silicon crystals has also increased dramatically and is summarized in Table 1.

Some of the challenges facing the crystal growth industry today are the ability of necks to support larger diameter crystals while successfully eliminating dislocations [18,19], thermal integrity of quartz crucibles and graphite purity. The author [20] has demonstrated the ability to eliminate dislocations with larger diameter necks (average diameter >10mm), in low resistivity boron doped crystals. This removes an important barrier in the progress towards even larger diameter (>400mm) crystals. Use of granular polysilicon is also expected to become a necessity for growth of larger diameter silicon crystals. Granular polysilicon helps with improving crucible integrity and also increasing crystal productivity [21].

Wafer Properties

Mechanical Properties:

Wafer flatness and plastic deformation are the two main mechanical aspects of the wafer that are critical to a device manufacturer. Wafer flatness directly affects its performance in photolithography [22]. The first ICs were patterned with contact printing, and wafer flatness did not pose a serious problem. The introduction of projection printing however resulted in massive changes. The patterned mask is now separated from the wafer and wafer flatness in the focal plane of the light beam (depth of focus) is crucial for uniform imaging in the photolithographic process. Wafer site flatness and related parameter requirements for DRAM and MPU applications are summarized in Table 2 [11]. One of the greatest challenges facing the silicon wafer industry today is achieving the flatness

levels projected by the roadmap. An added complexity to this problem is the limitation of currently available flatness measuring equipment to be able to measure accurately at these low levels [23].

Plastic deformation of wafers while assumed to have become a non-issue is again coming to the forefront with 300mm wafers [24]. Silicon wafer processing consists of multiple steps where the wafers are pushed into and out of high temperature furnaces. Typically, the wafers are arranged in a parallel row on a quartz boat with narrow spacing between the individual wafers. High rates of insertion and withdrawal of the quartz boat containing the wafers, into and out of the furnace, impose high thermal gradients on the wafers. If the radial temperature gradients are high enough, the resulting thermal stress can cause plastic deformation, and hence dislocation formation on the wafers.

The effects of temperature, dopant concentration and type, oxygen and nitrogen, on plastic deformation and dislocation mobility in silicon have been extensively studied in the literature [25-29]. Plastic deformation and dislocation mobility are always more severe in FZ silicon wafers compared to CZ silicon wafers [30,31]. The difference in behavior between the two types of wafers is explained by the difference in oxygen content. The oxygen atoms in CZ silicon create a Cottrell atmosphere [32] around the stationary or slowly moving dislocations thereby locking them firmly. This makes CZ silicon harder compared to FZ silicon, and more resistant to plastic deformation during device processing furnace operations.

Gettering:
Two types of gettering are used in silicon, internal and external [33]. External gettering involves creating gettering sites by external means, predominantly in the backside of the wafer. The sinks are created by mechanical damage, deposition of silicon nitride or polysilicon films or by deposition of a phosphorus glass layer in the back surface. By contrast, internal gettering relies on internal defects created by oxygen precipitation to create gettering sites.

Internal gettering is more prevalent today. Internal gettering was first introduced by Tan [9], to explain the improvement of leakage-limited yield of bipolar transistors in CZ silicon wafers. Prior to this, oxygen was considered a harmful impurity in CZ silicon due to the degradation in device yield that resulted from oxygen precipitates in the near-surface device region.

Internal gettering requires a super-saturation of oxygen. Oxygen precipitates and their associated defects are formed in the wafers by high temperature annealing of the wafers prior to device processing. Each device manufacturer uses a proprietary thermal cycle to precipitate an optimal number of gettering sites in the bulk of wafer, while creating a surface region (denuded zone) that is free of precipitates.

A novel method of accomplishing bulk internal gettering, with a wide well controlled denuded zone using a simple single step process has recently been reported [10]. This breakthrough has eliminated the black art associated with the control and behavior of

oxygen. It delivers a pre-programmed denuded zone depth (magic denuded-zone®) and internal gettering performance that is independent of the wafer's thermal history, oxygen concentration and the details of the crystal growth process, as shown in figure 1.

Metallic Impurities:
3d, 4d and 5d transition metals when present at large enough concentrations can affect electrical conductivity, but are more detrimental as recombination centers that reduce minority carrier lifetime [34]. Minority carrier lifetime strongly influences electrical device parameters like leakage current, switching behavior and storage time in MOS memories.

In the late forties, lack of availability of high purity materials imposed very short lifetimes on crystals, and hence devices fabricated on these substrates, showed poor performance. By the early fifties, lifetime for germanium was increased to 300-600 μsec, but it was much more difficult to get acceptably high values for silicon [3].

Device manufacturers today are aiming at a reduction of metal impurity levels to below 10^{10} cm^{-2} and the limits imposed on the silicon wafer manufacturers are even more stringent ($\leq 5x10^{9}$ cm^{-2}). Recombination lifetime is sensitive to Fe in boron-doped silicon even below 10^{10} cm^{-3}. On the other hand, extremely fast-diffusing metal impurities like Cu or Ni preferentially precipitate at the wafer surface to form silicides, which cause junction leakage in devices.

Intrinsic Point Defects:
Intrinsic point defects (vacancies and self-interstitials) were not a problem in silicon till the growth of dislocation-free crystals by Dash [2]. Dislocations within the crystal provided a suitable sink for the intrinsic point defects preventing their nucleation and agglomeration.

Swirl-type defects in dislocation free crystals were first reported by Abe et al. [4] in 1966. These swirl type defects were revealed as shallow pits by Sirtl etching. These defects were later classified as A and B-defects, based on their characteristics. Initially, based on work with metals, where vacancies are the dominant point defects, discussion of A and B-defects was directed at controlling vacancy reactions [35]. It was not until 1975, that A-defects were identified to result from self-interstitial condensation, and somewhat later for B-defects [36-38]. A-defects were shown to consist of extrinsic dislocation loops (or stacking faults), typically elongated in the <110> direction with a size of ~ 1-3 μm. Images of extrinsic dislocation loops observed by Föll et al. [37], are shown in Figure 2. These defects may consist of only a single dislocation loop or multiple dislocation loops. A-defects forms as an agglomeration of self-interstitials. A-defect nucleation is most likely heterogeneous. Carbon has been shown to influence A and B-defect formation.

Little is understood concerning the mechanisms associated with B-defect nucleation. Petroff and de Kock [39], obtained images of this defect, but did not analyze their structure. It has not been well characterized because of the weak strain field associated

with these defects. Unlike the A-defect, B-defects are not small dislocation loops, but a loose collection of silicon self-interstitials. Some type of impurity atom, most likely carbon is speculated to influence the formation of the loosely packed three-dimensional agglomerates. More work is needed to understand the formation and structure of these defects.

In 1981, Roksnoer et al. [5], identified a new type of defect in silicon crystals called the D-defect. The size, density and distribution of these defects was different from that of A and B-defects. Also, these defects could not be revealed by means of preferential etching or TEM, indicating they were not dislocations. They could only be observed by copper or lithium decoration, followed by X-ray topography.

It was only as late as 1996, that Itsumi et al. [40], were successful in imaging D-defects with TEM (Figure 3). Their work confirmed earlier speculations that D-defects are vacancy agglomerates in the shape of an octahedral void. The walls of the octahedron were (111) planes, with a thin oxide layer coating.

There is not too much mention of C-defects in the literature. Very little is known about these defects, except that it is somewhat smaller than a B-defect (< 800Å), and is occasionally observed between the B-defect region and defect free material and/or crystal surface [41].

Evolution of an engineered wafer

While the structure of the different silicon wafer defects and their impact on device yield had been studied for some time, not much was comprehended about the formation of these defects and the actual mechanism by which all of these defects degraded device yield. The 1990s have seen the biggest progress in these areas. It has resulted in a clearer picture of the relationship between crystal growing conditions and defect formation and the mechanism by which these defects contribute to early device failure.

De Kock looked at varying crystal growth rates in his investigation of A and B-defects, and observed the complete elimination of A-defects at a growth rate of 3mm/min [35]. Following the discovery of D-defects, Roksnoer et al. [5] identified more clearly the effect of crystal growth rate on the concentration and type of these intrinsic defects. Both and A and B-defects were observed at lower growth rates compared to D-defects and a defect-free regime was observed at intermediate growth rates, as shown in figure 4.

Voronkov [42], put a lot of these experimental observations on much firmer theoretical footing with his seminal paper in 1982. He identified the axial temperature gradient at the crystal-melt interface to be an equally important parameter along with crystal growth rate for formation of A, B and D-defects.

He introduced a parameter $\xi = V/G_z$ where V is the growth rate and G_z is the crystal axial temperature gradient, at the crystal-melt interface, that controlled the dominant point defect (vacancy or interstitial) that was grown into a crystal. If $\xi > \xi_{crit}$, vacancies were

the dominant point defects incorporated, if $\xi < \xi_{crit}$ interstitials were the dominant point defects incorporated (Figure 5). Based on experimental data on pedestal-grown crystals Voronkov estimated ξ_{crit} to be 3.3×10^{-5} cm^2/s °C.

It was not until 1996, however, that Voronkov's theory got wider acceptance by the silicon crystal growing community. Dornberger et al. [43], investigated the effect of position of the ring-like distributed oxidation induced stacking fault (OSF) in Czochralski grown silicon crystals as a function of crystal growth rate and axial temperature gradient at the crystal-melt interface. They showed that the radial position of the OSF ring could be predicted from an empirically found equation, $V/G(r) = 2.2 \times 10^{-5}$ cm^2/s °C, where r is the radial distance from the center of the crystal.

Crystal growth conditions and intrinsic point defect incorporation dynamics have been identified to influence more than just OSF ring formation and position. They control formation of low-density voids (also called Crystal Originated Particles) and dislocation clusters and they also influence oxygen precipitation behavior in the crystal [44].

The 1990s have also witnessed a more complete understanding of the mechanisms by which crystal grown-in defects influence device yield. Tachimori et al. [45], first noticed the effect of crystal growth rate on Gate Oxide Integrity (GOI), a parameter that relates to memory device performance. Simultaneously, a new type of "singularity" was observed following extended SC1 cleaning of silicon wafer surfaces by Ryuta et al. [46]. The defect was a shallow pit, 0.5μm in diameter and 0.06μm deep. The authors called these pits Crystal Originated Pits (COPs). Ryuta et al. [47], later observed that the size distribution of these pits was a function of crystal growth rate. These pits were linked to D-defects by Yamagishi et al. [48]. Park et al. [49-51], completed this picture with their finding that the presence of COPs in the gate oxide can lead to premature GOI failure.

Knowledge of the influence of silicon crystal growth conditions on defect formation and their effect on device yield have paved the way to engineer wafers that meet each device manufacturer's unique requirements. Complete elimination of agglomerated vacancy or interstitial type defects has also been achieved [44,50]. Engineering the appropriate amount of gettering behavior into the wafer [10], while maintaining a defect-free near surface region, provides the optimal combination of desired wafer properties (Figure 1). Thus, the birth of an engineered wafer!

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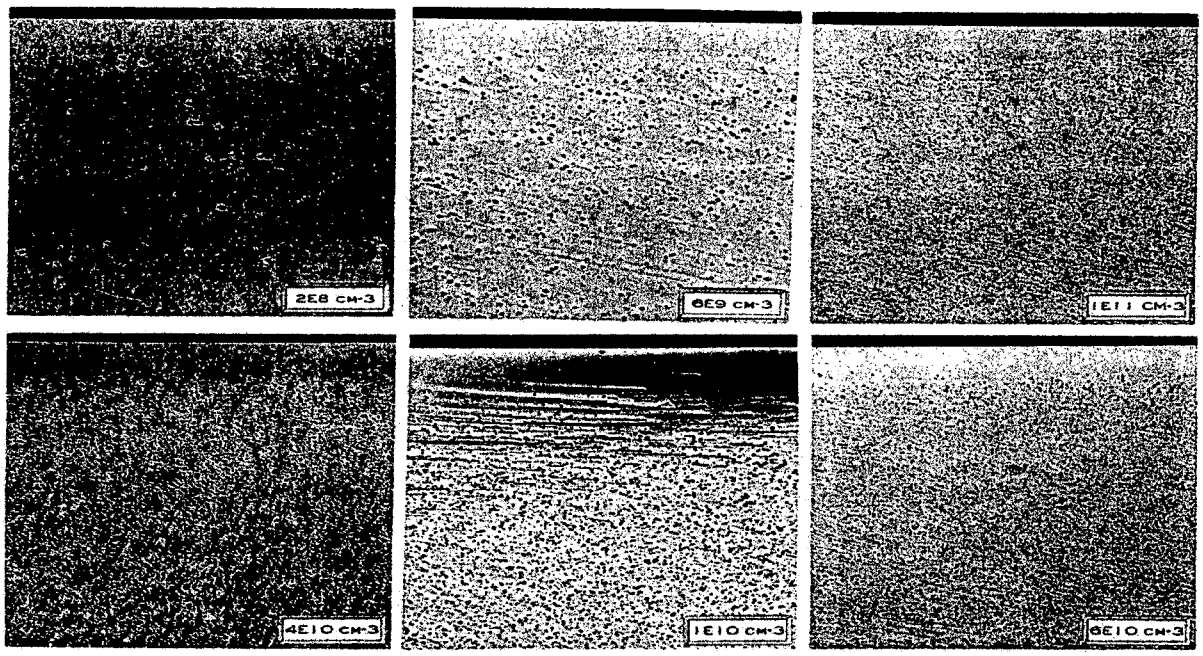
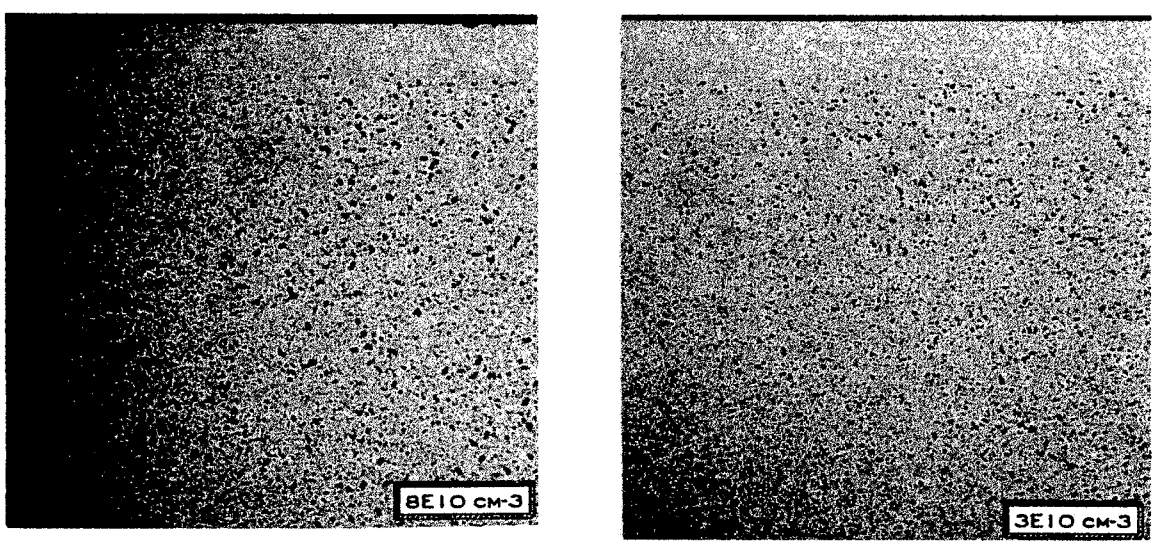
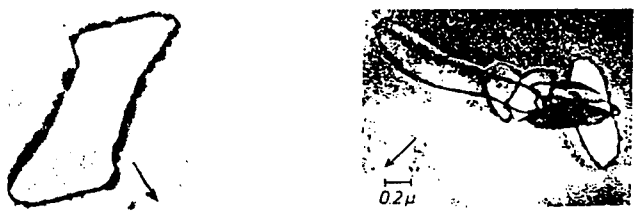


a) O_i = 12ppma O_i = 14ppma O_i = 16ppma



b) Seed-end wafer Opposite-end wafer

Figure 1: Application of Magic Denuded Zone™ Process on wafers with different initial oxygen levels and different thermal history. a) The pictures in the top row show the effect of conventional denuding and oxygen precipitation compared to pictures in the bottom row that show effect of MDZ. b) Shows the independence of oxygen precipitation and depth of precipitate to crystal thermal history with MDZ™.



a) b)

Figure 3: TEM images A-defects. a) A single dislocation-loop and b) Multiple dislocations-loops from Föll et al. [37]

Figure 4: TEM image of an octahedral void (D-defect), just below an oxide particle from Itsumi et al. [40]

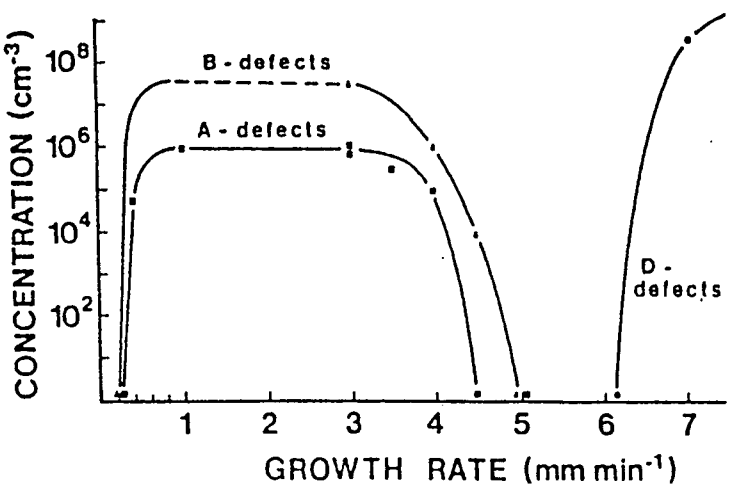


Figure 5: Concentration of A, B and D-defects as a function of growth rate in 23mm diameter pedestal-pulled silicon crystals from Roksnoer et al. [5]

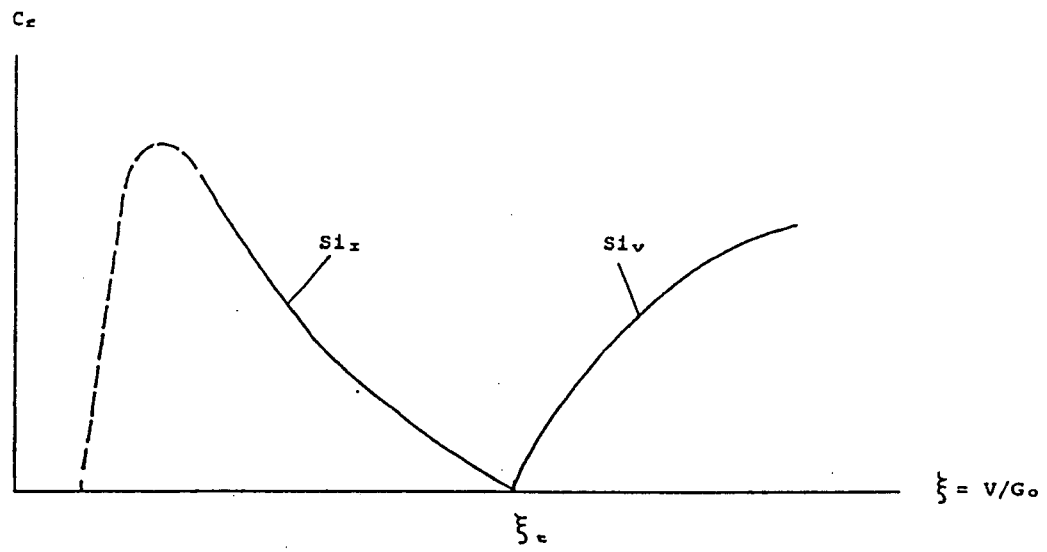


Figure 6: Survived point defect concentration C_f (either vacancy or interstitial), as a function of $\xi = V/G_z$, where V is the crystal growth rate and G_z, the crystal axial temperature gradient at the crystal-melt interface.

Table 1: Comparison of charge size, crucible diameter, puller height for different crystal diameters [52]

Crystal Diameter (mm)	**Charge Weight (kg)**	**Crucible Diameter (inches)**	**Height of Puller (feet)**
100 – 150	25 – 40	14 – 16	14
200	100 - 150	22 – 24	21
300	250 – 400	32 – 36	25
400	500 - 800	40 - 48	30

Table 2: Several Site Flatness and Related Parameters With Technology Generation [11]

Year of First Product Shipment	1999	2001	2003	2006	2009	2012
Technology Generation	180nm	150nm	130nm	100nm	70nm	50nm
Dense Lines (DRAM Half Pitch)*	180	150	130	100	70	50
Isolated Lines (MPU Gates)	140	120	100	70	50	35
Site Flatness (SFQR) (nm)	≤ 180	≤ 150	≤ 130	≤ 100	≤ 100	≤ 100
Site Size (mm x mm)	25 x 32	25 x 34	25 x 36	25 x 40	25 x 44	25 x 32
Site Area (mm^2)	800	850	900	1000	1100**	1300**
Depth of focus (μm, usable @ full field with ± 10% exposure)	0.7	0.6	0.6	0.5	0.5	0.5