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축전지 구동 응용을 위한 새로운 승압형 DC/DC 컨버터

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A New Current-Fed Isolated Boost Converter for Battery Powered Applications

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Abstract

A new isolated boost dc to dc convertor suitable for a low input voltage application is proposed. The proposed convertor features the low switch current stresses, the wide input voltage range operation, and the inherent inrush current protection characteristics, essential to design a low to high voltage conversion circuit. A comparative analysis and experimental results are presented to show the validity of the proposed convertor.

1. Introduction

In the electric vehicle applications where the input power is a low voltage source such as battery and the required output is a high dc voltage, there is a need to develop a high power density boost dc-dc convertor which features less complexity, compact size, and low cost. The major problem in developing such a convertor is that the convertor is suffered from high current stress and thus it is difficult to improve the overall power efficiency. To relieve this high current stress problem, the various dc-dc convertors have been proposed [1-3]. Among them, the dual convertor [1] seems to be attractive since it features less device current stresses compared to the other. However, it still shows high switch current stress and low efficiency and it is difficult to design to cope with wide duty cycle and input voltage range to improve the performance of the output regulation. Also, to solve the inrush input current problem at start up condition, which is the general case in all boost derived convertor, there needs a start up circuit such as start up resistor or clamp windings supported by diode [1,3], which also causes high cost and low efficiency. Thus, it is necessary to develop an efficient convertor operated with low switch stresses and wide duty cycle and input voltage range. Also, it should be included that the convertor can restrict the inrush current without any start up circuit for high efficiency and low cost. In this letter, a new convertor suited to low input voltage application is introduced. The proposed convertor, which does not need the start up circuit, gives the significantly reduced switch current stress and the extended duty cycle and input voltage range. A comparative analysis and experimental results are presented to show the validity. It is best suited in designing a simple, low cost, and high power density boost conversion circuit.

2. Operational principles

Fig.1 shows the circuit diagram of the proposed boost dc-dc convertor and its key waveforms. The proposed convertor of Fig.1 is composed of two switches S_1 and S_2, two diodes D_1 and D_2, an isolation transformer Tr, an output capacitor C_o, and two coupled inductors L_{c1} and L_{c2}. Each coupled inductor with the input to output coupled windings wound on the same core, has the same turn ratio as the isolation transformer, n. With the aid of these magnetic coupled windings, the convertor gives higher step-up input to output voltage conversion ratio than that of the dual convertor. Due to its higher step-up voltage conversion ratio, the current and voltage stresses of the switches S_1 and S_2 becomes small and it can operate with wide input voltage variation. The basic operation with the switch duty cycle $D \geq 0.5$ defined as shown in Fig.1, is described as follows. During the switches S_1 and S_2 ON interval ($t_0 \leq t < t_1$), since the voltage across the primary winding of the transformer Tr, v_p, becomes zero, the current flowing through it, i_p, also becomes zero. Since the dotted ends of two coupled inductors L_{c1} and L_{c2} are positive with respect to the undotted ends, the diodes D_1 and D_2 are reverse biased and the currents i_{D1} and i_{D2} are zero. Since the input voltage V_i is applied across the primary inductances L_{1p} and L_{2p}, their currents i_1 and i_2 increase linearly with the slopes of V_i / L_p, where it is assumed

that $L_{1p} = L_{2p} = L_p$. During the interval $t_1 \le t < t_2$, S_2 is turned *OFF*, while S_1 is still *ON*. Since the dotted end of L_{C1} is positive, the diode D_1 remains reverse biased and i_{D1} remains zero. The currènt i_1 increases as it does during the previous interval. However, since the current flowing through the primary winding of L_{C2} can not change instantaneously, the voltage across it reverses its polarity. As such, the dotted ends of L_{C2} are now positive, the diode D_2 is forward biased, and i_{D2} also flows. Moreover, since the dotted ends of Tr is now positive, the current i_p also can flow. The result is that the voltage v_p becomes $(V_i + V_o/n)/2$ and the voltage across L_{2p} becomes $(V_i - V_o/n)/2$ with respect to the undotted end during this interval. The energy stored in L_{2p} is transferred to the load through Tr and L_{2s}, respectively. Considering the power balance between L_{C2} and Tr, it is obvious that the current i_2 and the current i_p have the same amplitude, and the result is that i_2 at the instant t_1 becomes half the current at the instant just prior to t_1. The current flowing through the switch S_2, i_{S2}, becomes the sum of i_1 and i_2, and the voltage across the switch S_2, v_{S2}, becomes $(V_i + V_o/n)/2$ during this interval. During the interval $t_2 \le t < t_3$, both S_1 and S_2 are turned *ON* again and the convertor operation is the same as that during $t_0 \le t < t_1$. During the interval $t_3 \le t < t_4$, the diode D_1 is turned on and v_p now becomes $(V_i + V_o/n)/2$. The energy stored in L_{C1} is transferred to the load. At t_4, S_1 is turned *ON* and the another switching cycle starts.

It is noted that the proposed convertor can be operated even when $D \le 0.5$, since there exists a direct path that the stored energy in each coupled inductor during one switch *ON* interval can be transferred to the load during both switches *OFF* interval. This operation, termed as a buck mode operation, resembles that of a flyback convertor or a push-pull current-fed convertor with the start up circuit [2]. The inrush input current can be restricted in the proposed convertor as it does in the flyback convertor, simply by adopting the period of the buck mode operation at start up. Thus, the proposed converter can be designed without any start up circuit.

3. Analysis and comparison to dual convertor

Analysis is carried out with the assumption that all the parasitic elements are neglected and the primary inductance value L_p is large enough to neglect the current ripples. The dc-dc voltage conversion ratio, α, which can be derived by adopting the volt-second balance law to L_{C1} or L_{C2}, is expressed as $\alpha = \frac{V_o}{V_i} = \frac{n}{1-D}$. It is noted that V_o/V_i of the proposed convertor is always higher than $\frac{n^*}{1-D^*}$, that of the dual convertor where n^* and D^* are the turn ratio and duty cycle, respectively. Since the average currents of i_1 and i_2 have the value of $I_i/2$, the half of the input current, the flat-topped magnitudes of i_1 and i_2 shown in Fig.1, can be easily obtained from their current waveforms. Other flat-topped values such as peak switch current, peak diode current are also shown in Fig.1. Table 1 summarizes the comparison of the proposed convertor and the dual convertor. The device stresses are shown in Fig.2, in designing a $90W, 12V-150Vdc$ convertor with the conditions that $D = D^* = 0.613$. As can be seen in this figure, the values of the switch *rms* current and the transformer peak volt-ampere are significantly reduced. The peak value of the switch current is also reduced. Although the proposed convertor shows slightly higher *rms* current of the inductor, it is noted that the *rms* current of the switch of the proposed convertor is greatly reduced than that of the dual converter in the order about half time. Thus, it is expected that the proposed converter gives an improved efficiency in designing high power density boost convertor. Another advantage is that the proposed converter can be operated in a wider input voltage range. This can be easily obtained with the voltage conversion ratios of two convertors, $[V_o/V_i]_{proposed}$ and $[V_o/V_i]_{dual}$ including the parasitic resistance of the inductor r_L.

Fig.3 shows the plot of the input voltage as a function of the duty cycle in designing a $90W, 12V-150Vdc$ convertor with the conditions that $r_l = 0.0026R_o$. As can be seen, there exists the maximum duty cycle to control the convertors appropriately. Since D_{max} is higher than $D_{max}{}^*$, the proposed convertor gives more controllable duty cycle range to improve the regulation characteristics. The allowed minimum input voltage of the proposed convertor, $[V_{i\,max}]_{proposed}$, is $7.36Vdc$, whereas that of the dual convertor, $[V_{i\,max}]_{dual}$, is $10.9Vdc$. The allowed input voltage range is extended to about 60%, and thus, the proposed convertor can be controlled over the wide input voltage range.

4. Experimental results and conclusion

A $90W, 12-150Vdc$ prototype has been designed to varify the operation of the proposed convertor. The component values are $f_s = 50KHz$, $L_{1p} = L_{2p} = 100uH$, transformer and coupled inductor turn ratio $n = 3$, and $C_o = 220uF$. To limit the switch surge voltage, conventional *RCD* snubbers were adopted. Fig.4 shows the experimental results of the voltage and current waveforms at the rated condition.

The peak current of the switches is $7.0A$, and the transformer peak volt-ampere is measured as $1.08KVA$, which are the same results of Fig.2. It clearly shows that the waveforms are agree well with the theoretical analysis. The measured efficiency of the proposed convertor is 87% at full load, which is better than that of the dual convertor. Fig.5(a) shows the voltage and current waveforms of the switch with the conditions that Vi=8Vdc. The flat-topped voltage of the switch is 29V, the same result obtained from Table 1. Thus, it clearly shows that the proposed convertor can be operated near the theoretical limit of the minimum input voltage. Fig.5(b) shows the waveforms of the buck mode operation at start up. The waveforms resemble those of the push-pull current fed convertor with the start up circuit. Thus, it is obvious that the proposed convertor can restrict the inrush current. In a conclusion, as the proposed convertor features the high efficiency, the wide operation range, and inherent inrush current protection characteristics, it is best suited to design a low cost, high power density, low to high voltage conversion circuit.

References

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[2] V.J.Thattuvelil, T.G.Wilson, and H.A.Owen, "Analysis and design of a push-pull current-fed converter", Proceedings of the IEEE PESC, pp.192-203, 1980.

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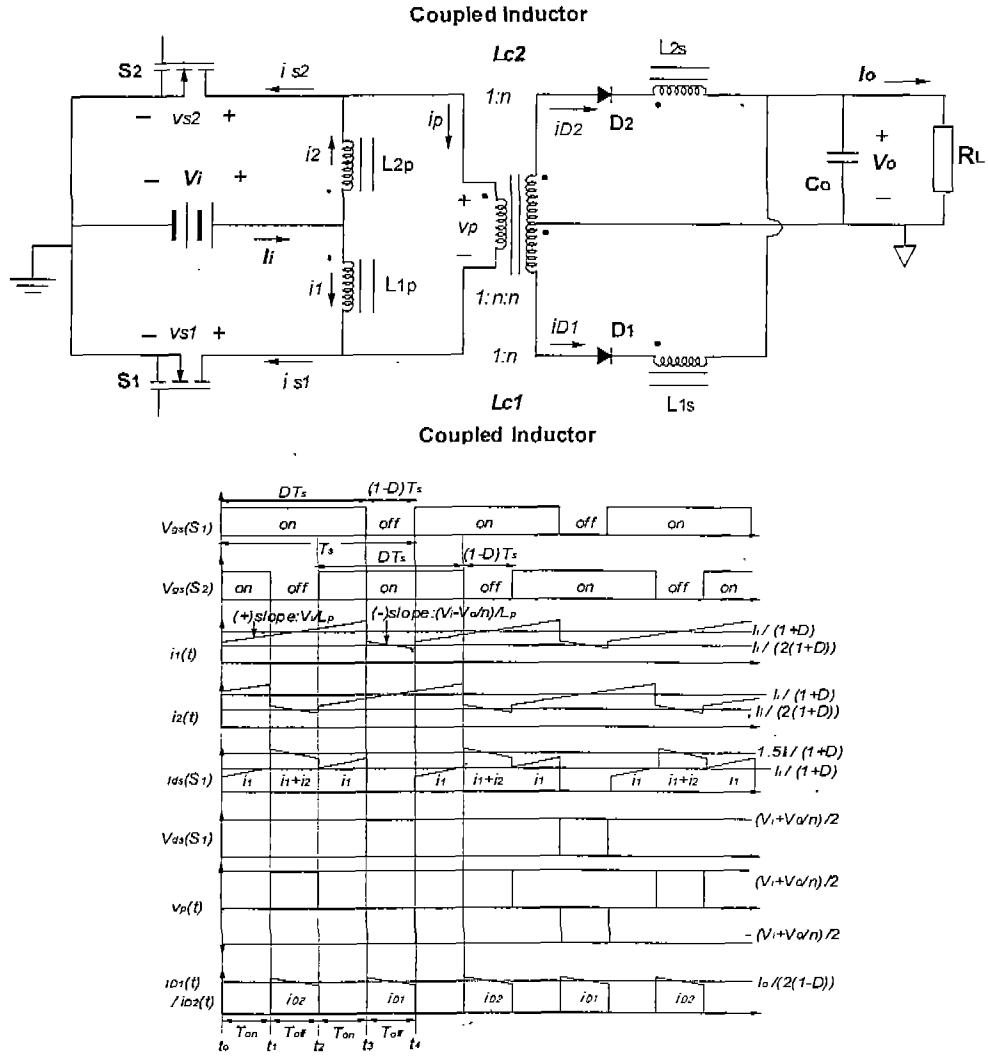

Fig.1. Circuit diagram of the proposed convertor and its key waveforms

Table 1. DC-DC convertor comparison

Device stress		Proposed convertor	Dual convertor
Voltage conversion ratio $\frac{V_o}{V_i}$		$\frac{n(1+D)}{1-D}$	$\frac{n^*}{1-D^*}$
Switch	peak current $I_{S,pk}$	$0.75(\alpha+n)I_o$	αI_o
	rms current $I_{S,rms}$	$\frac{I_o}{8}\sqrt{(\alpha+n)(4\alpha+6n)}$	$\frac{I_o}{2}\sqrt{\alpha(\alpha+2n^*)}$
	peak voltage $V_{S,pk}$	$\frac{V_i+V_o/n}{2}$	V_o/n^*
Diode	peak current $I_{D,pk}$	$\frac{I_o(\alpha+n)}{4n}$	$\frac{\alpha I_o}{2n^*}$
	rms current $I_{D,rms}$	$\frac{I_o}{2}\sqrt{\frac{\alpha+n}{2n}}$	$\frac{I_o}{2}\sqrt{\frac{\alpha}{n^*}}$
	peak voltage $V_{D,pk}$	nV_i+V_o	V_o
Inductor	dc current $I_{L,dc}$	$\frac{\alpha I_o}{2}$	$\frac{\alpha I_o}{2}$
	rms current $I_{L,rms}$	$\frac{\alpha I_o}{2}\sqrt{\frac{\alpha+n}{\alpha}}$	$\frac{\alpha I_o}{2}$
Transformer	volt-ampere Tr, pk	$\frac{n(\alpha+n)V_oI_o}{4}$	$\frac{\alpha n^* V_oI_o}{2}$
Capacitor	*rms* current $I_{C,rms}$	$I_o\sqrt{\frac{\alpha+n}{2n}}$	$I_o\sqrt{\frac{\alpha}{n^*}}$

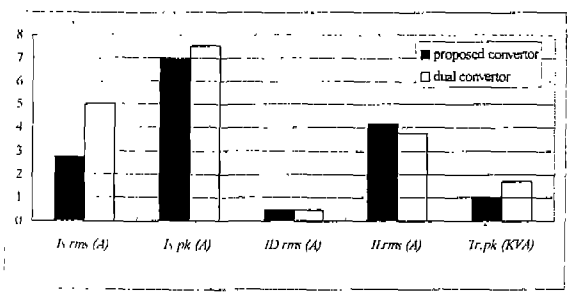

Fig.2. the device stresses

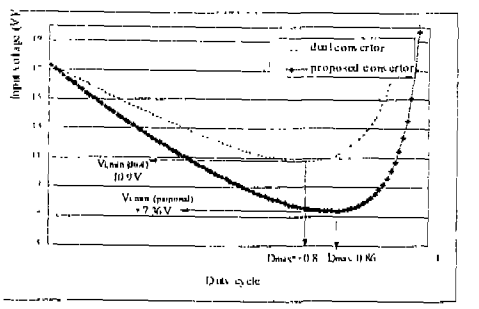

Fig.3. Allowable input voltage range

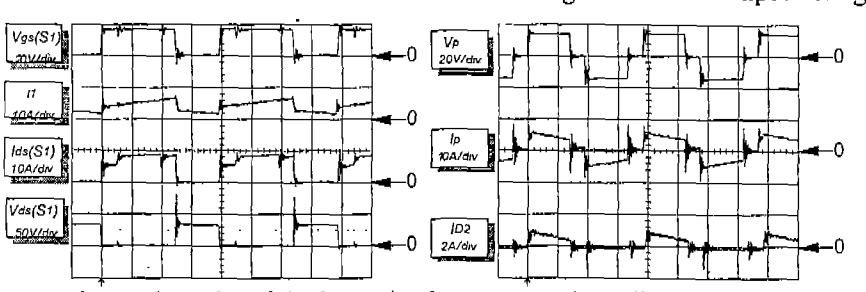

Fig.4. Experimental results of the key waveforms at rated condition (time: *5us / div*)

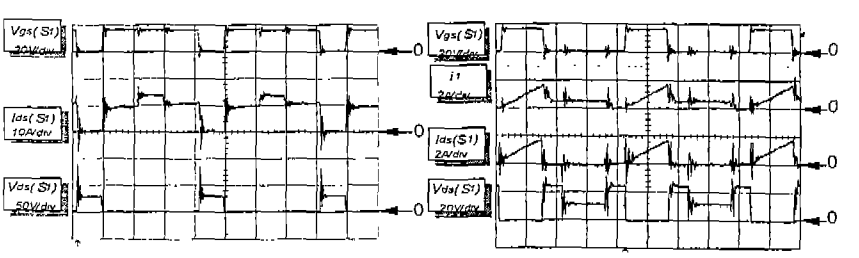

Fig.5. Experimental results of the key waveforms at rated condition (time: *5us / div*)