

능동 클램프 회로를 적용한 단상 ZCS 공진형 역률개선 컨버터

이준영, 문건우, 구관본, 윤명중

한국과학기술원

An Integrated Single-Stage Zero Current Switched Quasi-Resonant Power Factor Correction Converter with Active Clamp Circuit

Jun-Young Lee, Gun-Woo Moon, Gwan-Bon Koo, and Myung-Joong Youn

Department of Electrical Engineering
Korea Advanced Institute of Science and Technology

Abstract

A new integrated single-stage zero current switched(ZCS) quasi-resonant converter (QRC) for the power factor correction(PFC) converter is introduced in this paper. The power factor correction can be achieved by the discontinuous conduction mode(DCM) operation of an input current. The proposed converter has the characteristics of the good power factor, low line current harmonics, and tight output regulation. Furthermore, the ringing effect due to the output capacitance of the main switch can be eliminated by use of active clamp circuit.

I. INTRODUCTION

Recently, standards such as IEEE 519 and IEC 61000 impose a limit on the harmonic current drawn by equipments since conventional off-line power supplies including the full-bridge diode rectifier generate highly distorted input current waveforms with large amount of harmonics. In low power applications, these requirements must be satisfied in single stage to reduce the size and cost[1]. Most of single stage converters developed for this purpose adopt the PWM control which prevents the increase of the switching frequency

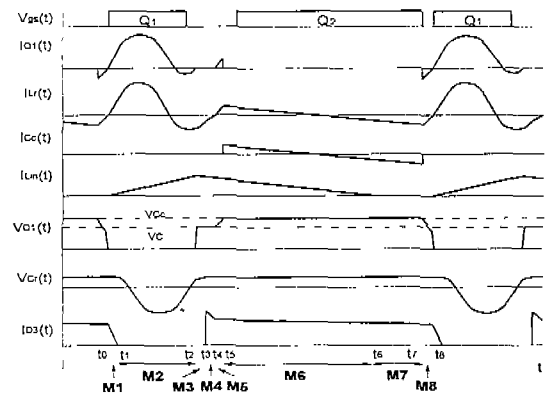


Fig. 2 Key waveforms for mode analysis

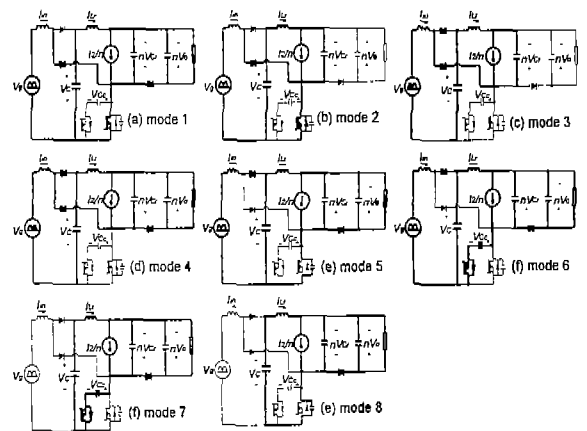


Fig. 3 Operational mode diagrams

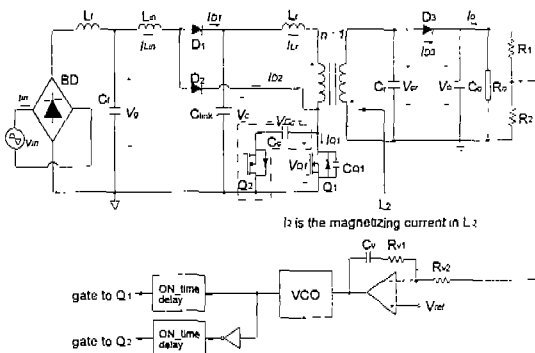


Fig. 1 Schematic of the proposed converter

due to the switching losses. To solve this problem, small number of papers have suggested single stage resonant DCM PFC converters but they have disadvantages of input current waveform distortion at zero-crossing-points and a large low frequency output voltage ripple[2],[3]. In this paper, single-stage ZCS QRC power factor corrector based on flyback topology operating in DCM. This converter gives a good power factor, improved input current waveform without distortion at zero-crossing-points, and tight output

regulation. In general, switching component of ZCS QRC suffers from additional voltage stress due to a serious ringing during off-state. Thus, by adoption of active clamp circuit in the proposed converter, the ringing effect can be eliminated[4].

II. MODE ANALYSIS

Fig. 1 shows the circuit diagram of the proposed converter with an conventional single output voltage loop. The basic structure can be understood as a cascade connection of a boost converter followed by a flyback QRC and these converters share the same switch. An active clamp circuit for eliminating the ringing effect is shown in dotted line. As shown in Fig. 2, each switching period is subdivided into eight modes and their topological states are shown in Fig. 3.

Mode 1 ($t_0 < t \leq t_1$)

Mode 1 begins at t_0 when the switch Q_1 is turned on. Since the resonant inductor current, $I_L(t)$, is smaller than the magnetizing current reflected to the transformer primary, I_2/n , the rectifying diode, D_3 , maintains on-state and the resonant capacitor voltage, $V_C(t)$, is clamped to the output voltage, V_o . Where, n means the transformer turns ratio. Thus, $I_L(t)$ is linearly increased and can be expressed as

$$I_L(t) = \frac{V_C + nV_o}{L_r}(t - t_0). \quad (1)$$

Also, the input inductor current is linearly increased with the slope of V_g/L_{in} as follows:

$$I_{Lm}(t) = \frac{V_g}{L_{in}}(t - t_0), \quad (2)$$

which continues until the end of mode 2. This mode stops when $I_L(t)$ reaches I_2/n .

Mode 2 ($t_1 < t \leq t_2$)

The rectifying diode, D_3 , is reverse biased as the resonant capacitor discharges its energy to the resonant inductor. The voltage across the resonant capacitor, $V_C(t)$, decreases sinusoidally as

$$\frac{dV_C(t)}{dt} = \frac{I_2}{C_r} - \frac{nI_L(t)}{C_r} \quad (3)$$

and the rate of increase of the resonant current becomes

$$\frac{dI_L(t)}{dt} = \frac{V_C}{L_r} + \frac{nV_C(t)}{L_r}. \quad (4)$$

The resonant inductor current and the input inductor current flow together into the switch Q_1 and this switch current, $I_{Q1}(t)$, will continue to oscillate and feed energy back to the link capacitor until time t_2 .

Mode 3 ($t_2 < t \leq t_3$)

Mode 3 begins after Q_1 is turned off at t_2 . Since the current flowing in the resonant inductor cannot change

abruptly, the diode D_2 is forced to be on-state to make the path for $I_L(t)$ and the diode D_1 also starts to conduct to transfer the energy charging in L_m to the link capacitor. Thus, the resonant capacitor, C_r , is charged by $I_L(t)$ reflected to the transformer secondary through D_1 and D_2 as well as I_2 . From the mode diagram shown in Fig. 3(c) the differential equations can be written as follows:

$$\frac{dI_L(t)}{dt} = \frac{nV_C(t)}{L_r} \quad (7)$$

$$\frac{dV_C(t)}{dt} = \frac{I_2}{C_r} - \frac{nI_L(t)}{C_r}. \quad (8)$$

Since the switch Q_1 is turned off after mode 2, $I_{Lm}(t)$ begins to be linearly decreased as follows:

$$I_{Lm}(t) = \frac{V_g - V_C}{L_{in}}(t - t_2) + \frac{V_g}{L_{in}}(T_{d1} + T_{d2}). \quad (11)$$

where T_{d1} and T_{d2} mean the durations of modes 1 and 2, respectively. This mode stops when $V_C(t)$ is equal to V_o .

Mode 4 ($t_3 < t \leq t_4$)

When C_r is charged to the point which D_3 is forward biased at t_3 , the output bulk capacitor is connected to the resonant capacitor in parallel and $V_C(t)$ is clamped to V_o , which results in the linear increase of $I_L(t)$ as shown in eqs. (12) and (13):

$$I_L(t) = \frac{V_o}{nL_r}(t - t_3) + I_L(t_3) \quad (12)$$

$$V_C(t) = V_o \quad (13)$$

where $I_L(t_3)$ is the initial condition of mode 3. Since $I_L(t)$ reflected to the transformer secondary and the magnetizing current flow together into the load, the powering mode is initiated. Until the energy held in L_r is fully transferred to the output stage, both D_1 and D_2 keep conducting. Therefore, as can be seen in the mode diagram, the drain-source voltage of the switch Q_1 is equal to the link voltage during modes 3 and 4.

Mode 5 ($t_4 < t \leq t_5$)

At the zero-crossing instant of $I_L(t)$, D_2 is blocked and a new resonant network is formed between L_r and C_{Q1} as shown in Fig. 3(e). The resonant inductor current, $I_L(t)$, and the drain-source voltage of Q_1 , $V_{Q1}(t)$, increase with the following rates:

$$\frac{dI_L(t)}{dt} = \frac{(V_C + nV_o)}{L_r} - \frac{V_{Q1}(t)}{L_r} \quad (14)$$

$$\frac{dV_{Q1}(t)}{dt} = \frac{I_L(t)}{C_{Q1}} \quad (15)$$

with the initial condition of $I_L(t_4) = 0$ and $V_{Q1}(t_4) = V_C$. When $V_{Q1}(t)$ reaches to V_{C_c} , the next mode begins.

Mode 6, 7 ($t_5 < t \leq t_7$)

Once $V_{Q1}(t)$ increases to the point where the antiparallel diode of Q_2 begins to conduct, $V_{Q1}(t)$ is clamped to the clamp voltage. During mode 6 and 7, the clamp capacitor current, $I_{Cc}(t)$, flows in a resonant manner by the clamp capacitor, C_c , and the resonant inductor, L_r . This can be expressed as follows:

$$I_{Cc}(t) = I_{Lr}(t_5) + \frac{V_C + nV_o - V_{Cc}}{L_r} (t - t_5) \quad (18)$$

where $I_{Lr}(t_5) = \sqrt{(nV_o)^2 - (V_C + nV_o - V_{Cc})^2} / Z_Q$. During mode 6, $I_{Lm}(t)$ decreases to zero with the same slope of mode 3 and D_1 is blocked.

Mode 8 ($t_7 < t \leq t_8$)

The auxiliary switch, Q_2 , is turned off at t_7 and the resonant inductor, L_r , resonates with the output capacitance of Q_1 , C_{Q1} . During this small dead time, the energy stored in L_r discharges some quantity of the energy stored in C_{Q1} .

III TURN-ON TIME OF Q_2

In order to guarantee the operation of mode 3, 4, and 5, Q_2 must not be turned on prior to the end of mode 5. Also, to discharge the energy of the clamp capacitor, Q_2 , must be turned on before the clamp capacitor current reverses its direction. Since the time durations are varying under line and load conditions, ΔT_{Q2} , which is defined as the dead time after Q_1 is turned off, should satisfy

$$\max \left\{ \sum_{i=1}^5 T_{di} - T_{Q1} \right\} \leq \Delta T_{Q2} \leq \min \left\{ \frac{T_{d6} + T_{d1}}{2} \right\} \quad (19)$$

where T_{Q1} is the pulse width of the gate signal of Q_1 . This condition happens when the line voltage has a peak value at a full load.

IV. DESIGN

A. Selection of L_{in} and n

To determine L_{in} , a steady state analysis must be performed in advance. By averaging the large signal model equations half a line cycle, the solutions of V_C and V_o become

$$V_C = \frac{V_{grms}}{\sqrt{2}} \left(1 + \sqrt{1 + \frac{0.852n^2 \eta R_o (1 - d_{fs})^2}{L_{in} d_{fs} f_r}} \right) \quad (20)$$

$$V_o = \frac{d_{fs}}{1 - d_{fs}} \frac{V_C}{n} \quad (21)$$

where $d_{fs} = f_s / f_r$. From above two equations, the transformer turns ratio can be founded as:

$$n = \frac{\sqrt{2} L_{in} f_r V_o V_{grms} d_{fs}}{L_{in} f_r V_C^2 (1 - d_{fs}) - 0.426 V_{grms}^2 \eta R_o (1 - d_{fs}) d_{fs}} \quad (22)$$

To maintain a sinusoidal line current, the input inductor current must flow in DCM over entire line cycle. This requirement is guaranteed by the following condition as

$$\frac{\sqrt{2} V_{grms}}{V_C - \sqrt{2} V_{grms}} d_{fs} \leq 1 - d_{fs} \quad (23)$$

With eqs. (20), (21), and (23), the maximum L_{in} to meet DCM can be calculated as follows:

$$L_{in} \leq \frac{0.426 d_{fs} \eta R_o V_{grms}^2}{f_{ss} V_C^2} \quad (24)$$

Once L_{in} is calculated using eq. (24) and design specifications at the worst case, the transformer turns ratio, n , can be obtained using eq. (22).

B. Selection of L_r and C_r

During mode 2, the switch current is written as

$$I_Q(t) = \frac{I_2}{n} + \frac{1}{Z_r} (V_C + nV_o) \sin \omega_r (t - t_1) + \frac{V_C}{L_{in}} (t - t_1 + T_{d1}) \quad (25)$$

In order to achieve a ZCS condition over the entire line cycle, the switch current must be zero at the end of mode 2 when the line voltage has a peak value. This can be written as follows:

$$\frac{I_2}{n} + \frac{1}{Z_r} (V_C + nV_o) \sin \zeta + \frac{\sqrt{2} V_{grms}}{L_{in}} \left(\frac{\zeta}{\omega_r} + T_{d1} \right) = 0 \quad (26)$$

where ζ is defined as $\omega_r T_{d2}$. This equation may be satisfied when ζ has a value between π and 2π . It is necessary to select a suitable due to the heavy current stress of switch, which is the general characteristic of a ZCS QRC. Eq. (26) clearly shows that a current stress of the switch becomes minimal when the characteristic impedance Z_r satisfying a given resonant frequency is selected as large as possible and this condition can be accomplished if ζ has the value of $3\pi/2$. Thus eq. (26) is rewritten as follows:

$$\frac{I_2}{n} - \frac{1}{Z_r} (V_C + nV_o) + \frac{\sqrt{2} V_{grms}}{L_{in}} \left(\frac{3\pi}{2\omega_r} + T_{d1} \right) = 0 \quad (27)$$

Therefore, L_r and C_r are determined from eq. (27), and a desired resonant frequency in rad/sec, ω_r , at a full load condition.

C. Selection of C_c

To prevent the ringing across Q_1 when Q_1 is turned off, the resonant frequency formed by C_c and L_r should be sufficiently low. On the other hand, if too large a value of C_c is chosen, it may be bulky and costly. Therefore, a good design guideline has been suggested that the capacitor value is selected so that one half of the resonant period formed by C_c and L_r exceeds the maximum off time of Q_1 [9]. This can be expressed as follows:

$$C_c \gg \frac{(1 - d_{fs, min})^2}{\pi^2 L_r f_{ss, min}^2} \quad (28)$$

D. Selection of Switches

Assuming that the clamp capacitor is selected sufficiently large, the voltage stress of switches Q_1 and

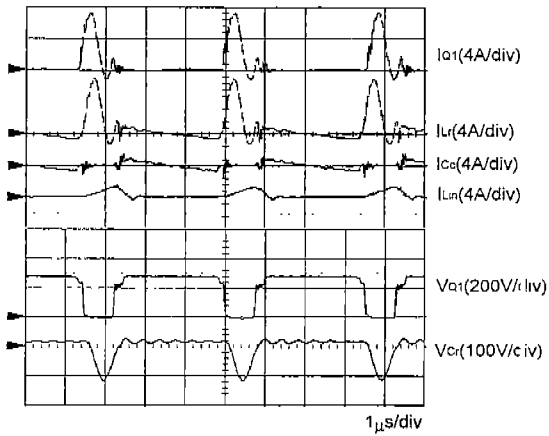


Fig. 4 Experimental key waveforms

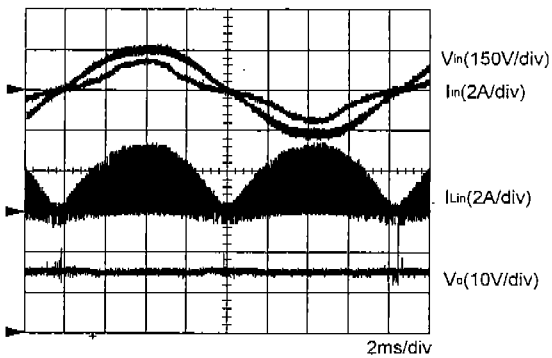


Fig. 5 Experimental waveforms of V_{in} , I_{in} , I_{Lin} , V_o

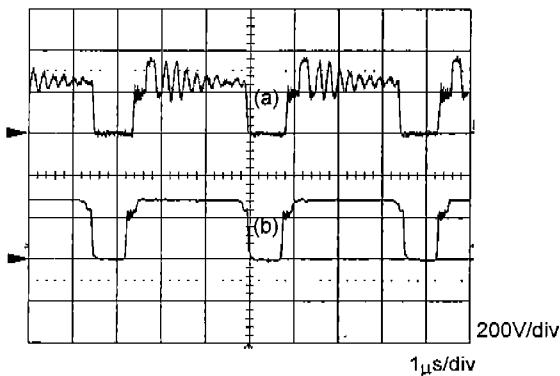


Fig. 6 VQ1 with RCD clamp ($R=20k\Omega$, $C=10nF$) (a) and active clamp (b)

Q_2 are approximately expressed as following equation:

$$V_{Q1,2} \approx V_C + nV_o. \quad (29)$$

The worst case of voltage stress happens at a light load. Thus, the maximum voltage stress can be found using eqs. (20) and (29) with $R_o=R_{o,max}$ and $f_{ss}=f_{ss,min}$. Also, the worst case of current stress of Q_1 happens at a full load and the peak line voltage. The peak current stress can be expressed as

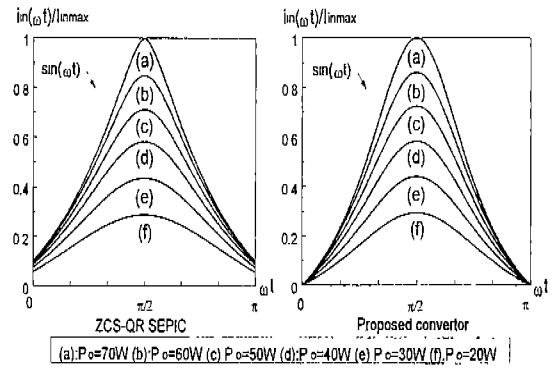


Fig. 7 Normalized line current waveforms in a half cycle as a function of load

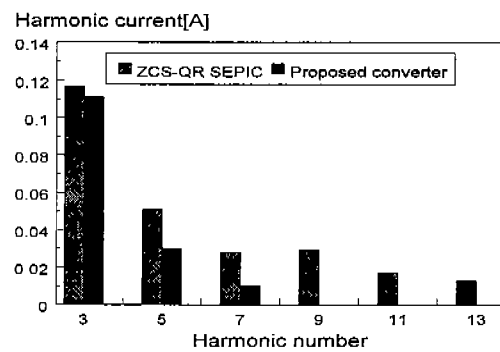


Fig. 8 Harmonic currents of ZCS-QR SEPIC and the proposed converter at $P_o=70W$

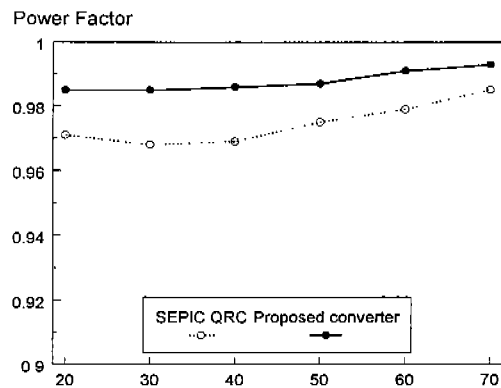


Fig. 9 Power factor of ZCS-QR SEPIC and the proposed converter

$$I_{Q1pk} = \frac{\sqrt{2} V_{g,rms}}{L_{in}} \left(-\frac{\pi}{2\omega_r} + T_{d1} \right) + \frac{I_2}{n} + \frac{1}{Z_r} (V_C + nV_o). \quad (30)$$

V. EXPERIMENTAL RESULTS

The prototype converter has been constructed to show the operation of the proposed converter based on the design equations with $V_g=110V_{rms}$, $V_o=15V$, $P_o=70W$, $f_r=1.25MHz$, $f_{s,max}=300kHz$, and $\eta=85\%$.

Using the design equations given in section V, the

Table 1 Parameter Lists

L_f	80 μ H	Q_1, Q_2	IRFP450
L_r	9 μ H	D_1, D_2	D5L60
C_f	0.1 μ F	D_3	FML36S
C_r	34nF	BD	D6SB60L
C_c	1 μ F	$n:1$	4.3:1
C_o	1000 μ F	ΔT_{Q2}	1 μ s

converter parameters are selected as listed in Table 1. Figs. 4 and 5 show key waveforms of the proposed converter. As can be seen in these figures, the switching waveforms are well agreed with theoretical analysis and the filtered line current follows the line voltage with low line current distortion at line zero-crossings while the output voltage is tightly regulated. Fig. 6 is the experimental waveforms of drain-source voltage of Q_1 with RCD clamp and active clamp circuit. This figure shows that the drain-source voltage of Q_1 can be clearly clamped by the active-clamp circuit, which results in the reduction of additional voltage stress caused by the ringing effect. To show the advantages of the proposed converter, some comparisons are made with ZCS-QR SEPIC. Fig. 7 shows the normalized input current waveforms of ZCS-QR SEPIC and the proposed converter as a function of load for one half-cycle. This figure shows that the line current of the proposed converter does not have an offset at the line zero-crossing and it is more close to the sinusoidal waveform than the line current of ZCS-QR SEPIC. The measured harmonic currents are shown in Fig. 8. Fig. 9 shows the plot of the power factor as a function of output power in the two converters. As can be seen in this figure, due to the lower THD of the proposed converter compared with that of ZCS-QR SEPIC, the power factor of the proposed converter stays more higher. Finally, the efficiency of the proposed converter is plotted in Fig. 10. This figure shows that this converter has the efficiency of about 87% at the rated condition.

VI. CONCLUSIONS

This paper has presented the analysis, design, and experimental results of an integrated ZCS QRC for PFC operating in DCM. By eliminating the distortion of the line zero-crossings in the line current waveform, THD and power factor can be improved. Since the proposed converter is capable of producing the desired output voltage without a significant output voltage ripple, it is possible to carry out the tight and fast output voltage regulation with a wide bandwidth output voltage

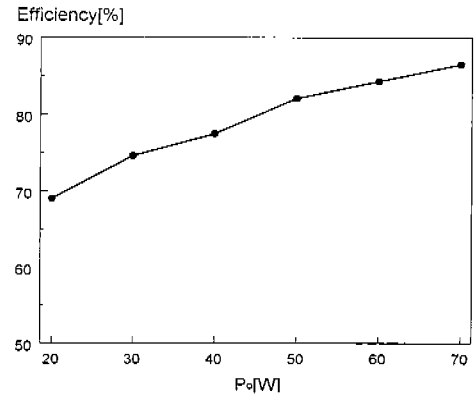


Fig. 10 Efficiency of the proposed converter

controller while not degrading the line current waveform. In addition, the voltage stress caused from the ringing effect can be reduced by using active clamp method while achieving ZCS of the main switch. The prototype converter gives a high power factor of above 0.985, low THD, and a high efficiency of 87%. Therefore, the proposed converter is expected to be suitable for a compact power converter with a tightly regulated output voltage requiring a switching frequency of more than several hundreds kHz.

REFERENCES

- [1] M. Madigan, R. Erickson, and E. Ismail, "Integrated high quality rectifier-regulators," in *IEEE Power Electronics Specialist Conf.*, 1992, pp. 1043-1051.
- [2] D. Balocco, and C. Zardini, "The half-wave quasi-resonant ZCS flyback converter as an automatic power factor preregulator : An evaluation," in *IEEE Applied Power Electronics Conf.*, 1996, pp. 138-144.
- [3] J. Sebastian, J. A. Martinez, J. M. Alonso, and J. A. Cobos, "Voltage-follower control in zero-current switched quasi-resonant power factor preregulators," *IEEE Trans. Power Electron.*, Vol. 13, no. 4, pp. 727-738, 1998.
- [4] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," in *IEEE Power Electronics Specialist Conf.*, 1994, pp. 909-916.