멀티레벨 인버터 및 컨버터를 위한 새로운 저손실 스너버

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A New Generalized Undeland Snubber Circuit for Multilevel Inverter and Converter

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Abstract - This paper proposes a new snubber circuit for multilevel inverter and converter. The snubber circuit makes use of Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber. The proposed snubber keeps such good features as fewer number of components, improved efficiency due to low loss snubber, capability of clamping overvoltage across main switching devices, and no unbalance problem of blocking voltage. Furthermore, the proposed concept of constructing a snubber circuit for multilevel inverter and converter can apply to any kind of basic snubber unit such as Holtz nondissipative snubber, McMurray efficient snubber, Lauritzen lossless snubber, etc which have been utilized for two-level inverter.

1. Introduction

Recently the multilevel inverter and converter have drawn tremendous interest for high voltage and high power applications [1]-[7]. The general structure of the multilevel inverter and converter is to synthesize sinusoidal voltage waveforms from several levels of voltages typically obtained from capacitor voltage sources. As the number of levels increase, the synthesized output waveform adds more steps, producing staircase waveform which approaches the sinusoidal wave with minimum harmonic distortion. More levels also mean that higher DC link voltage than voltage rating of device itsef can be handled by series device without device voltage sharing problem and without the use of bulky and heavy transformer for multiple connections.

Until now, for multilevel inverter and converter, conventional RCD and RLD snubber as turn-off snubber and turn-on snubber, respectively, have been used widely and exclusively as shown in Fig. 1 because it is easy to apply to multilevel inverter and converter [6]-[7]. But this kind of snubbers need separate snubber circuit unit for each GTO which are composed of turn-off capacitors, turn-on inductors, resistors and diodes. Thus the total number of snubber components become considerably high and complex, thus resulting in highly costly multilevel inverter and converter. And since the large amount of snubber energy is fully dissipated in snubber

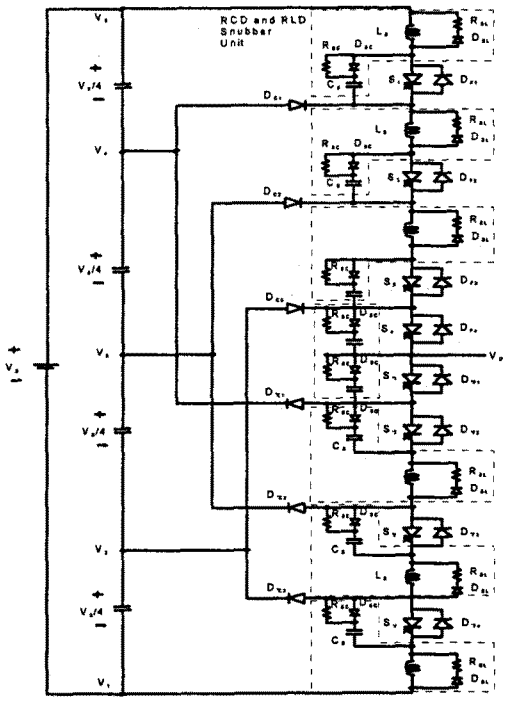

Fig. 1 Five-level inverter with conventional RCD/RLD snubber(within the dotted line).

resistor, system power loss can be very high, which causes system efficiency to become very low. Furthermore, during turn-off process, the overvoltage of GTO can be very high, usually about 1.8 times higher than DC link voltage because there is only one small turn-off capacitor for each GTO to absorb the stored inductor energy. In addition, unbalance problem of the overvoltage, which results from combination of multilevel structure and RCD/RLD snubbers, makes voltage stresses of the switching devices worse[7].

To overcome the above-mentioned disadvantage of RCD/RLD snubber for multilevel inverter and converter, a new snubber topology suitable for multilevel inverter and converter are proposed. The proposed snubber utilizes Undeland snubber as basic snubber unit and can be regareded as a generalized Undeland snubber for multilevel

structure converter. Its good features include fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and no unbalance problem of blocking voltage. This paper also explains in detail how to construct a snubber circuit for multilevel inverter and converter and simulational results of the new converter are included.

2. The Proposed Snubber for Multilevel Inverter and Converter

An m-level multilevel inverter typically consists of m-1 capacitors on the DC bus and produces m-levels of the phase voltage. Fig. 2(a) shows one pole of five-level inverter in which the DC bus consists of four capacitors, C_1, C_2, C_3, and C_4. For a DC bus voltage V_S, the voltage across each capacitor is $V_S/4$ and each device stress will be limited to one capacitor voltage level, $V_S/4$, through clamping diodes. Table 1 lists the voltage levels and their corresponding states. State condition 1 means the switch is on, and 0 is off. There exist four complementary switch pairs in each phase The complementary switch pair is defined such that turning on one of the pair switches excludes the other from being turned on. In case of five-level inverter, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4') which, respectively, correspond to each level change, that is, between V_5 and V_4, V_4 and V_3, V_3 and V_2, and V_2 and V_1. Notice that the level changes occur only between adjacent levels. When investigating all level changes, we can find the operating part of circuit during each level change to converge to equivalent two level inverter which is composed of complementary pair switches and corresponding clamping diodes. For example, as shown in Fig. 2, consider level changes between V_3 and V_4. The corresponding complementary pair is (S_2, S_2'). If S_2 is on and S_2' is off, output level is V_4. Convesely, If S_2 is off and S_2' is on, output level is V_3. During these level changes the operating components of five-level inverter can be drawn with thick line as shown in Fig.

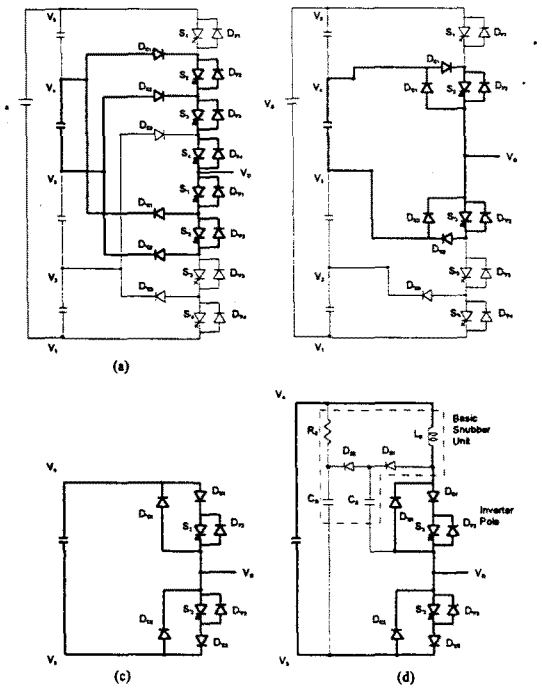

Fig. 2 Derivation of the proposed snubber for multilevel inverter (a)the operating part of circuit (thick line) during level changes between V4 and V3 , (b) Redrawn circuit of (a), (c)Equivalent two-level inverter during level changes between V4 and V3 , (d)Equivalent two-level inverter with a basic snubber unit.

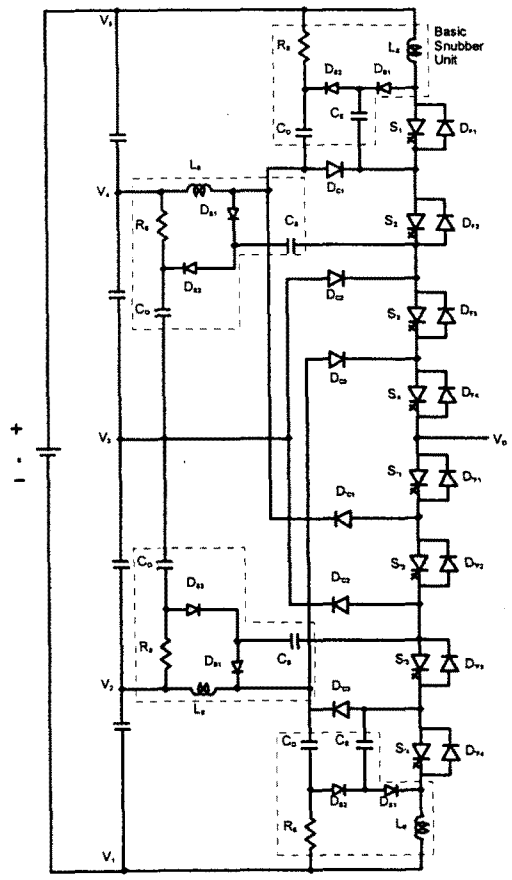

Fig. 3 Five-level inverter with the proposed snubber.

2(a). The thick-lined part of operating circuit can be transformed into Fig. 2(b) and can also be redrawn as Fig. 2(c) since switches S_3, S_4, and S_1' are always turned on irrespective of on/off condition of S_2 and S_2'. Fig. 2 (c) shows that the operating part of circuit is equivalent to the conventional two-level voltage source inverter. It follows that for the equivalent two-level inverter related to switching devices (S_2, S_2'), the basic snubber unit which have been used in two-level inverter can be applied as shown in Fig. 2(d). In the same way, all the equivalent two-level inverter corresponding to each level change, that is, each complementary pair in multilevel inverter can be derived, and the same basic snubber units can apply to them. So, we can obtain five-level inverter equipped with a snubber circuit as shown in Fig. 3. When using the same principle, we can get the snubber circuits for 3-level, 4-level. Furthermore, a generalized snubber for any multilevel inverter and converter can be achieved. The generalized snubber has the same good features as the basic snubber unit. In this paper since we use the Undelnand snubber[8] as the basic snubber unit, the characteristics of the generalized snubber are such as fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and easy arrangements and mounting of snubber circuit. Furthermore thanks to the snubber structure, the generalized snubber has no unbanlance problem of overvoltage unlike RCD/RLD snubber, thus resulting in equal voltage stress to all main switching devices except clamping diodes.

3. Conclusion

This paper proposes a new snubber circuit for multilevel inverter and converter. The snubber circuit makes use of Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber. The proposed snubber keeps such good features as fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and no unbalance problem of blocking voltage. Furthermore, the proposed concept of constructing a snubber circuit for multilevel inverter and converter can apply to any kind of basic snubber unit such as Holtz nondissipative snubber[9], McMurray efficient snubber[10], Lauritzen nondissipative snubber[11], etc which can be utilized for two-level inverter.

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Table 1

Five-level inverter voltage levels and corresponding switch states

Output	Switch State							
V_O	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_5=V_S$	1	1	1	1	0	0	0	0
$V_4=3V_S/4$	0	1	1	1	1	0	0	0
$V_3=2V_S/4$	0	0	1	1	1	1	0	0
$V_2=V_S/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

(1 : On , 0 : Off)