# 비선형 다중채널 Loudness 교정을 위한 고성능 보청기 칩

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# High-performance Digital Hearing Aid Processor Chip with Nonlinear Multiband Loudness Correction

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## ABSTRACT

Owing to technical advances in very large-scale integrated circuits (VLSI), high-speed digital signal processing (DSP) chips become fast enough to allow for real-time implementation of hearing aid algorithms in units small enough to be wearable. In this paper, we present a digital hearing aid processor (DHAP) chip built around a general-purpose 16-bit DSP core. The designed DHAP performs a nonlinear loudness correction of 8 octave frequency bands based on audiometric measurements. By employing a programmable DSP, the DHAP provides all the flexibility needed to implement audiological algorithms. In addition, the has a low power feature and 5.410x5.720 $mm^2$ dimensions that fit for wearable devices.

## 1. INTRODUCTION

For human being, 'hearing' is more than a mere sensory mechanism. With a loss of hearing, man is restricted from his or her normal social activity, which may in turn cause undesirable influence on mental health [1]. In order to compensate for this kind of handicap, lots of research have been conducted, most of which were focused on developing aid devices [2,3,4]. Recently, more challenging and fundamental biological approach such as cochlea implant method was proposed [2].

Modern hearing aids can be subdivided into three groups: analog, digital, and analog/digital hybrid hearing aids. Though majority of currently available hearing aids are analog devices employing conventional analog circuits, digital technology has offered new possibilities for noticeable advances of hearing aids. Using the digital technology, it is possible to add powerful features to the aids, such as nonlinear amplification, noise reduction, and enhanced fitting algorithms. There are also ongoing efforts in developing further advanced signal processing techniques for hearing aids. However, the size and computational capacity of the digital equipment have limited their use for the hearing impairment in comparison with the analog techniques. Owing to technological progress in very large-scale integrated (VLSI) circuits, high-speed digital signal processing (DSP) chips become fast enough to allow for real-time implementation of the hearing aid algorithms in units small enough to be wearable.

This paper concerns the designing of a digital hearing aid processor (DHAP) chip being operated by a dedicated DSP core. The DHAP for hearing aid devices must be feasible within size and power consumption required. Furthermore, it should be able to compensate for wide range of hearing losses and allow a sufficient flexibility for the algorithm development. The DHAP designed here meets the requirements addressed above. The chip performs 33 MIPS at 33MHz system clock with 3V power supply, and has the dimensions of 5.410x5.720 $mm^2$ fitted to wearable hearing aid devices. To compensate for wide range of hearing losses, a Nonlinear Multiband Loudness Correction (NMLC) algorithm is developed and implemented in the DHAP. The developed DHA algorithm and DHAP are described in Section 2 and Section 3, respectively.

## 2. DIGITAL HEARING AID ALGORITHM

Hearing loss can be classified into three categories; conductive loss, sensorineural loss and combination of both. The most obvious feature of impaired hearing is the shift in auditory threshold. Another feature often associated with the sensori-neural-type hearing impairment is the nonlinearity, so-called the loudness recruitment [1], i.e., the inability of the patient to perceive any sound at low to moderate sound-pressure levels and a steep increases from moderate to high. To confront those problems, therefore, dynamic compression circuits have traditionally been incorporated in hearing aids. They operate on full range of the input frequency or several independent frequency bands in order to account for the frequency dependence of the hearing dysfunction. Until recently, a variety of multiband signal processing algorithms have been proposed and tested [2,3,4]. Whilst some have failed, others have shown great improvement in

speech recognition scores.

For the development of the DHAP, a nonlinear multiband loudness correction (NMLC) algorithm is implemented. Processing steps for the NMLC

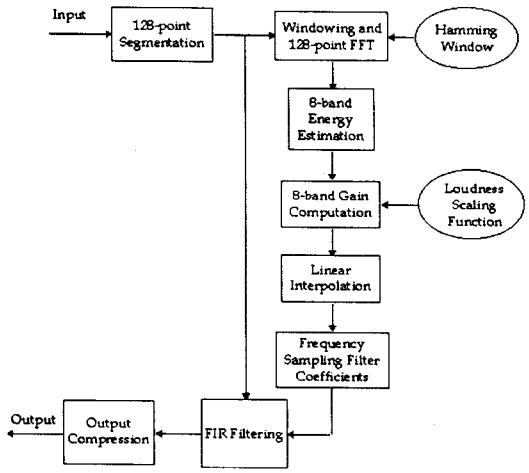


Figure 2. Gain computation from the LSF.

algorithm are illustrated in Figure 1.

Spectrum estimation procedures are used to estimate the energy of input signals. It should be mentioned that hearing loss functions are generally measured using narrow band signals and the incoming sounds consist mainly of broadband signals. To account for the loudness perception of the input complex sounds, the acoustic energy, rather than the magnitude, is measured.

The energy is estimated in eight frequency bands centered at 250, 500, 1.5K, 1K, 2K, 3K, 4K and 6KHz's, respectively. Thus, to attain the best performance of the algorithm, it is desirable to measure the hearing impairment of the patient for the same 8 frequency bands. Critical band channels were considered to determine those center frequencies. Total 19 critical band channels were grouped into 8 bands, each of which contains two or three critical bands. The input signal is sampled at the rate of 12 KHz, and segmented into windowed blocks of 128 samples without overlap. The 128-point Hamming window is used for the segmentation. Each block is then transformed into the frequency domain via FFT. The input energy for each frequency band is obtained by adding up the powers of all FFT coefficients belonging to the corresponding frequency band.

The acoustic amplification is done by filtering the input signal with the 128-tap length FIR filter. Frequency gain of the FIR filter is determined by the loudness scaling method that utilizes a function describing how much gain is needed for each frequency band to restore normal loudness perception. The loudness scaling function (LSF) is obtained from the difference between the loudness perception of normal listeners and that of impaired listener. Figure 2 shows how the gain factor is computed using the LSF. In the figure the input SPL is denoted by 'x' and the correspond-ing gain

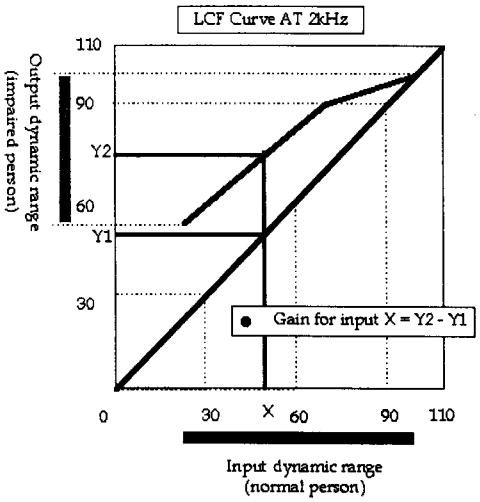


Figure 2. Computation of the gain using the LSF.

is 'Y2-Y1' that is set to produce output SPL of 'Y2'. The same process proceeds to the next band and continues until the gain computation for 8 frequency is completed.

Later, the gain factors for 8 frequency bands are interpolated using the linear interpolation method to obtain 128 frequency coefficients evenly distributed on the linear frequency axis. With them the 128-tap FIR filter is designed using the frequency-sampling method [5]. Since the gain factors are computed for every input frame, the frequency response of the FIR filter also changes in every 128 input samples, i.e., 10.7 msec time period. Thus, the gain factors are low pass filtered to produce smoother output signal.

A real-time software is designed using the SSP1605 assembly language to implement the NMLC algorithm described above. The SSP1605 DSP core is a 16-bit fixed point processor. More details on the SSP1605 can be found in User's Guide [6].

| PROCEDURE | PROM SIZE | CYCLES |
|---|---|---|
| Initialization | 38 words | 11,317 |
| Energy Estimation | 1,859 words | 27,196 |
| Gain Computation | 624 words | 3,017 |
| Filter Design | 388 words | 40,217 |
| FIltering & Output Compression | 476 words | 22,174 |
| ISR | 96 words | 7,622 |
| TOTAL | 3,643 words | 100,226 |

Table 1. Summary of the real-time software.

In summary, the software consumes 100K clock cycles to implement the algorithm, which corresponds to 9.4 MIPS complexity. Since the SSP1605 core is able to perform 33 MIPS at 3M Hz system clock when the 3V power is supplied, it uses only 28% of its maximum computational power. Table 1 summarizes the computational load

and memory usage. As can be seen from the table, 4K word program ROM and 1K word internal RAM were used to implement the NMLC algorithm in real-time.

## 3. DESIGNING OF THE DHAP CHIP

The DHAP is based on a general-purpose 16-bit DSP core SSP1605. The processor is composed of six units: DSP core unit, external peripheral interface unit (EPIU), codec interface unit (CIU), serial EEPROM memory interface unit (SEPMIU), and universal asynchronous receiver-transmitter (UART) interface unit (UIU). Figure 2 shows the schematic diagram of the DHAP.

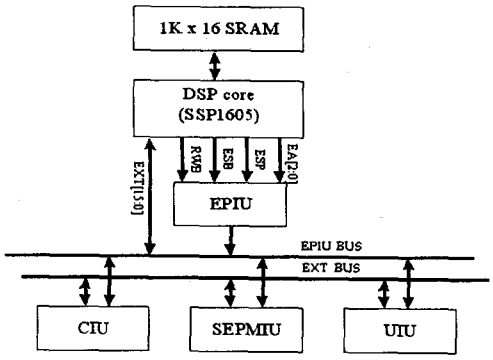


Figure 3. Schematic diagram of the DHAP.

The core unit comprises SSP1605 core, 4K word program ROM and 1K word data RAM. Though the DSP core can perform 33MIPS at 33M Hz system clock, 12.288 MHz clock is applied to the core because the computational power required by the NMLC algorithm is less then 10 MIPS. This approach enables one to reduce the power consumption of the DSP core.

The EPIU controls interrupt access of external peripherals such as codec, EEPROM, and UART. The CIU was designed to support a 16-bit single-channel S-D audio codec AD73311. End of conversion generated by the codec is to be connected to Interrupt 2 of the DSP core. Complying with the interrupt, the DSP collects input samples for one-frame (128 sample) period, during which it processes previous 128 samples. A 2K bit serial EEPROM was employed to store the loudness scaling function having the size of 7x8 words. The SEPMIU provides a path between the EEPROM and the DSP to read or write parameters in the EEPROM. In the real-time program, the table in the EEPROM is copied onto the internal RAM in the DSP core unit *prior to* the main operation. In such a way, the LSF is accessible without time delay.

Whenever requested, the DHAP should allow for the change of LSF parameters, in order to provide the impaired person with the best fitting. To meet this requirement, the UART interface unit (UIU) has been built in the processor. When the parameter change is required for fitting, the program running on a PC sends out parameters through RS232C port. The parameters are then written onto the EEPROM by the DSP through the UIU.

Figure 3 shows the internal architecture of the DHAP chip fabricated with 0.65 m double metal process. The fabricated DHAP has dimensions of 5.410x5.720 mm2 that is small enough to fit for wearable hearing aids. Moreover, the chip features a low operation power manageable with small batteries.

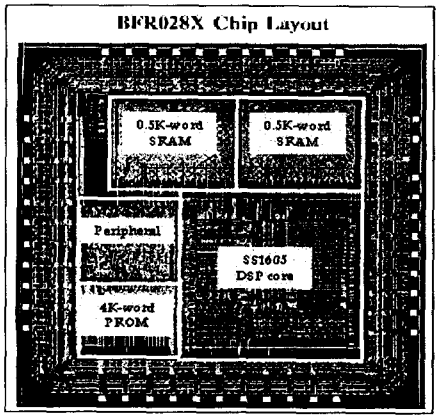


Figure 4. Internal architecture of the DHAP chip

## 4. CONCLUSIONS

A digital hearing aid processor chip built around a 16-bit DSP core was developed. Main features of the designed DHAP are described by the algorithms based on the nonlinear dynamic compression and high performance being achieved with low power consumption. In addition, the chip has the dimensions fit for wearable hearing aids. Using the chip, a body-worn type hearing aid has been developed and its electrical as well as clinical performances are currently under evaluation.

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