Investigations of Pd based hybrid ohmic contacts to high-low doped n-type GaAs

Hong Koo Baik, Joon Seop Kwak

School of Materials Science and Engineering, Yonsei University,
Seoul 120-749, Korea

Abstract - To improve electrical properties and uniformity of high-low doped n-type GaAs, new ohmic contacts with a low-resistance and the superior uniformity was developed using a concept of hybrid ohmic contact. The hybrid ohmic contact displayed good surface and interface morphology and had minimum contact resistivity of $3 \times 10^{-6}\ \Omega cm^2$ in a wide annealing temperature ranged from 340℃ to 420℃, which was much wider than that of conventional ohmic contacts. The microstructural analysis showed that the Pd/Ge/Ti/Au contact formed a nonspiking Pd/Ge ohmic contact at low annealing temperature (~300℃) and also produced an alloyed AuGe contact at high annealing temperature (~400℃), resulting in hybrid ohmic contacts.

I. Introduction

GaAs has been investigated and exploited for high speed digital and analog devices as well as optoelectronic applications[1]. Currently, high frequency power MESFETs operating at low voltages have been actively sought for high performance cellular phone and personal communication system[2]-[4].

Recently, high-low doped channel structure grown by molecular beam epitaxy (MBE) was demonstrated in developing a low-voltage-operating GaAs power MESFET[4]. The advantages of this structure are low gate capacitance, high gate-to-drain breakdown voltage, and uniform and high transconductance with gate bias in the device operation. In developing a device with high performance, low-resistance ohmic contact to the high-low doped n-GaAs is essentially needed, because this allows a low knee voltage and minimizes dissipation of power, with resulting increased efficiency and lower operating temperatures.

Alloyed AuGeNi ohmic contacts are commonly used as ohmic contacts to n-GaAs with a contact resistivity in the low-$10^{-6}\ \Omega cm^2$ range[5]. However, AuGeNi contacts have a rough surface and thermal instability during subsequent fabrication processes[6], which cause non-uniformity in electrical properties. To overcome the problems, nonspiking Pd/Ge ohmic contacts have been developed based upon the concept of solid-phase regrowth using n-GaAs/Pd/Ge system[7]. The contacts yield low contact resistivity, smooth surface and good edge definition. However, the Pd/Ge ohmic contacts also have problems that the contact resistance degraded one order of magnitude after isothermal annealing for 5 h at 400℃ and the process-window for rapid thermal annealing (RTA) is narrow, which results in large

variation of contact resistance in a wafer[7]-[8].

In this work, we focus on the enhancement of electrical properties and uniformity of high-low doped n-type GaAs through development of new ohmic contact having thermal stability, low-resistance, and good uniformity of contact resistance. For this purpose, we design new ohmic contact systems with a concept of hybrid contacts and elucidate the formation mechanism of the hybrid ohmic contacts.

Ⅱ. EXPERIMENTAL PROCEDURES

A layer structure for ohmic contact resistance measurements was formed by MBE on 3 inch semi-insulating (100)-oriented GaAs wafer. The structure consists of a 1μm thick undoped buffer layer in which GaAs/AlGaAs superlattices were introduced, a thin active layer doped to mid-$10^{17}cm^{-3}$ (high doped layer), a thick active layer doped to mid-$10^{16}cm^{-3}$ (low doped layer), and an undoped GaAs layer for surface passivation. Top layer of the undoped GaAs has a role of protecting the active layer from the surface defects created by oxygen chemisorption[9].

The ohmic contact resistivity (Rc) were measured using the transmission line method (TLM) where interspacing between metal pads were 5, 10, 15, 20, 30, 40, and 50μm. TLM test structures were defined by patterning photo-resist and chemical etching using H_3PO_4:H_2O_2:H_2O solution.

Prior to metal deposition, the GaAs surface was cleaned by dipping into HCl:H_2O, followed by a de-ionized water rinse and N_2 dry. A layered structure of ohmic metals was evaporated sequentially using an electron beam

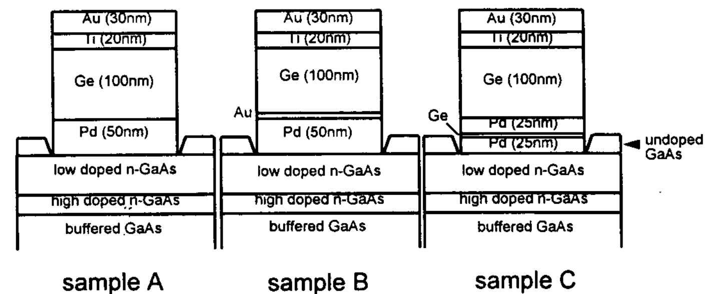

Fig. 1. A schematic cross-sectional illustration of samples A, B, and C.

under 1×10^{-6} Torr. Cross sections of the samples are shown schematically in Fig. 1. In the samples, the thickness of the Pd and Ge layers are chosen such that, upon annealing, the entire layer of Pd is consumed in the formation of PdGe, with excess Ge remaining, and followed by deposition of Ti/Au layers for produce hybrid contacts. For sample B, a thin Au layer is sandwiched between Pd and Ge layers in order to generate more Ga vacancies in the GaAs substrate through the interaction between the Au layer and Ga. For sample C, a thin Ge layer is added into Pd layer to supply more dopants in the GaAs substrate.

After the metal deposition, the photoresists were lifted off. The samples were annealed by rapid thermal annealing(RTA) method in N_2 ambient at the temperature range of 300-500℃ for 20 s.

Ⅲ. RESULTS AND DISCUSSION

A. Electrical properties of the hybrid ohmic contacts

Figure 2 shows variation of contact resistivity as a function of annealing temperature for the three samples. A typical U-shape dependence of the contact resistivity on the annealing

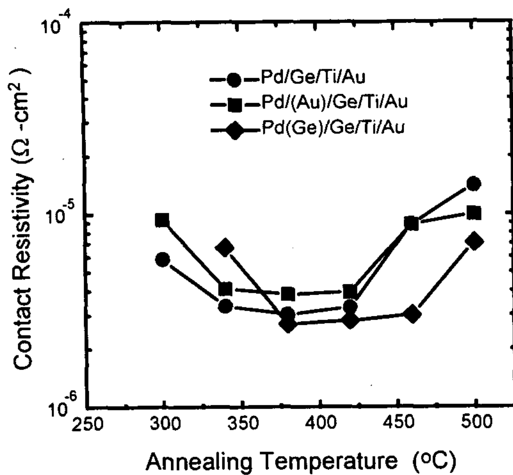

Fig. 2. Variation of contact resistance as a function of annealing temperature for samples A, B, and C.

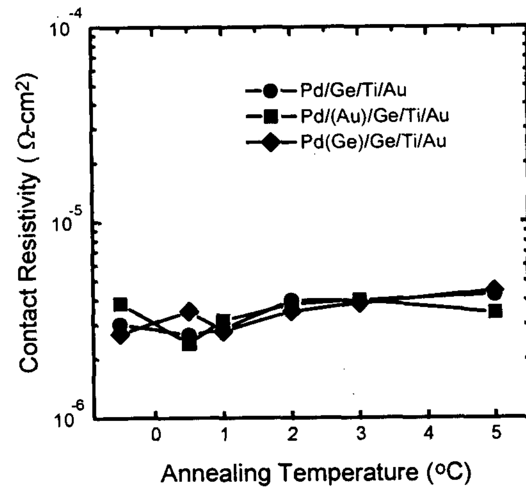

Fig. 3. Changes of contact resistances of samples A, B, and C during isothermal annealing at 400℃. The initial annealing condition was 380℃ for 20 s.

temperatures was obtained[10]. For sample A, the Rc decreases with increasing the annealing temperature from 300 to 340℃, and is almost constant at 3.0×10^{-6} $\cdot \Omega cm^2$ in a wide annealing temperature ranged from 340 to 420℃. Figure 2 clearly indicates that the minimum contact resistivity of sample A is two times lower than that of previously reported nonspiking Pd/Ge contact ($\sim 7 \times 10^{-6} \Omega cm^2$)[11]. Further increase in annealing temperature results in the increase of contact resistivity.

The addition of the thin Ge layer (sample C) reduced the minimum contact resistivity to 2.6×10^{-6} Ωcm^2, while the thin Au layer (sample B) increases the minimum contact resistivity to 3.8×10^{-6} Ωcm^2. Figure 2 indicates that the hybrid contacts developed in this work displayed low contact resistivity in a wide temperature range.

The thermal stability for samples A, B, and C were investigated using isothermal annealing at 400℃. The contact resistances are shown in Fig. 3 as a function of annealing times. The contact resistivities are almost unchanged even after annealing for 5 h at 400℃. Note that the thermal stability of the samples is much better than that of previously reported Pd/Ge ohmic contacts[7].

B. Formation mechanism of hybrid ohmic contacts

In order to elucidate the formation mechanism of the Pd based hybrid ohmic contacts, we investigated the the role Ti layer deposited between Pd/Ge and Au through the comparison among Pd/Ge/Au, Pd/Ge/Mo/Au, and Pd/Ge/Ti/Au contacts. When the layer was absent (i.e. Pd/Ge/Au contact), a ohmic contact with high contact resistance was formed only at high annealing temperature of 460℃. When Mo was added between Pd/Ge and Au (i.e. Pd/Ge/Mo/Au contact), an ohmic contact was produced only at low annealing temperature of 300℃. In case of Ti (i.e. Pd/Ge/Ti/Au contact), an ohmic contact with a wide-process-window ranging from 340 to 420℃ was obtained with a low-resistance. Auger depth profile and X-ray diffraction results showed that the Pd/Ge/Au

contact and the Pd/Ge/Mo/Au contact were produced by alloyed AuGe contact and nonspiking Pd/Ge contact, respectively, while the Pd/Ge/Ti/Au contact was formed by both the Pd/Ge contact and the AuGe contact through appropriate control of Au indiffusion by Ti. When the annealing temperature was lower than 300℃, ohmic contact was formed through solid phase regrowth of GaAs doped with Ge (Pd/Ge contact). When the annealing temperature was above 340℃, the ohmic contact was produced through the formation of AuGa, followed by generation of free electrons by the incorporation of Ge into the Ga vacancies. This resulted in the low-resistance hybrid Pd/Ge/Ti/Au ohmic contact with a wide-process-window. From these results, appropriate control of Au indiffusion by Ti was essential to the formation of the Pd based hybrid ohmic contacts.

For further elucidation of the formation mechanism of the hybrid ohmic contacts, interfacial microstructures of Pd/Ge/Ti/Au ohmic contact to GaAs were investigated using cross-sectional transmission electron micro-scopy (XTEM), and their results were used to interpret the electrical properties. Figure 4 shows XTEM micrographs of three samples: as-deposited, and annealed separately at 300℃ and at 380℃ for 20s. Annealing at 300℃, as shown in Fig. 4(b), yielded the layer structure of GaAs/PdGe/Au_4Ti/Ti oxide. The ohmic contact was formed through a solid phase regrowth of GaAs heavily doped with Ge below the PdGe layer. At 380℃, the layer structure was changed to GaAs/(Ge-Ti-As)/PdGe/(TiO_2, As_2O_3), as shown in Fig. 4(c). Spikes composed of Au and AuGa were found at the grain boundaries of the PdGe compound. The formation of AuGa at 380℃ reduced the contact resistance through the creation of more Ga vacancies at the interface of GaAs/PdGe, and the incorporation of elemental Ge. In addition, formation of AuGa through fast indiffusion of Au toward GaAs substrate allowed the contact to be formed directly on the buried high-doped GaAs layer, which eliminated the resistance due to low-doped GaAs layer and the high-low resistance, with resulting further reduction of contact resistance.

Figure 5 shows an energy-band diagram of

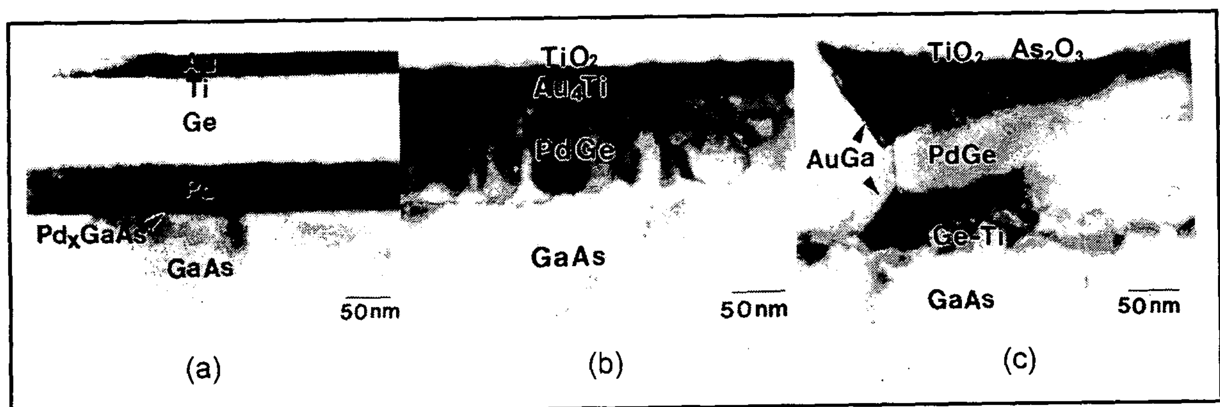

Fig. 4. Bright-field XTEM micrograph of the hybrid Pd/Ge/Ti/Au contact under three conditions : (a) as-deposited state, (b) annealed at 300℃ for 20s, and (c) annealed at 380℃ for 20s.

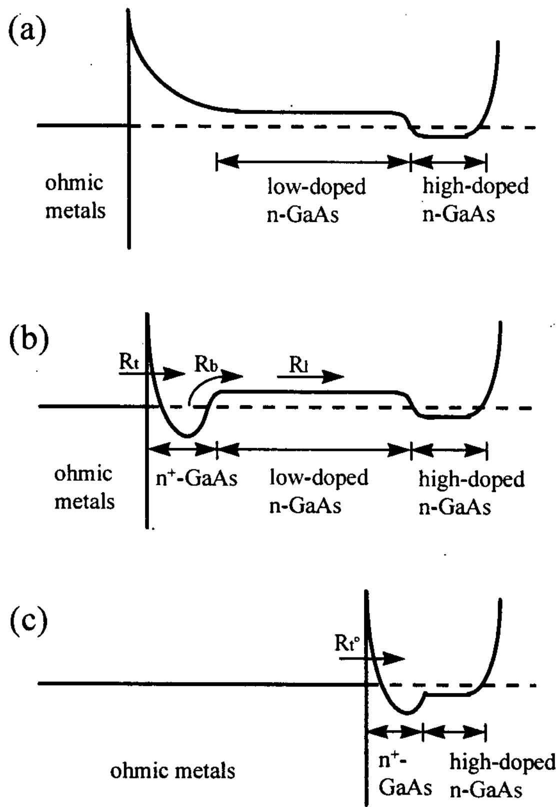

Fig. 5. Energy-band diagrams for samples (a) in the as-deposited state, (b) annealed at 300℃ and (c) annealed at 380℃. The contact is formed on the surface of low-doped GaAs after annealed at 300℃. It directly contacts the buried high-doped GaAs layer at 380℃.

the n-GaAs/contact deduced from the electrical and microstructural analysis. In the as-deposited state, the Schottky barrier with a thick depletion layer and high barrier is formed at the n-GaAs/contact interface[12], which prevents the formation of an ohmic contact in the as-deposited state. Figure 5(b) shows the change in the energy-band diagram after annealing at 300℃. The depletion layer width and height of the Schottky barrier is reduced considerably by the presence of the n^+-GaAs layer, followed by tunneling of carriers through the barrier. This results in the formation of an ohmic contact at 300℃. n^+-GaAs is produced as follow: a thin metastable Pd_xGaAs layer is formed at low temperature, as shown in Fig. 4(a), and excess Ge for the formation of PdGe causes it to decompose, resulting in regrowth of the Ge-doped n^+-GaAs layer[7].

When the contact is formed at the surface of the low-doped GaAs layer due to shallow penetration, as shown in Fig. 5(b), three resistance sources are produced between ohmic metals and the buried high-doped GaAs layer: resistance due to tunneling through the Schottky barrier (R_t), resistance due to a high-low barrier (R_b), and resistance due to a low-doped GaAs layer (R_l). The deep penetration to the high-doped GaAs layer, as shown in Fig. 5(c), eliminates the resistance due to the low-doped GaAs layer, resistance due to the low-doped GaAs layer, which allows the conduction band minimum to be lower than the Fermi level. This removes the high-low resistance. Thus, when the contact is formed directly on the buried high-doped GaAs layer, only tunneling resistance remains, which reduces contact resistance at 380℃. In addition, the formation of AuGa, as shown in Fig. 4, is also responsible for the low contact resistance obtained at 380℃. The formation of AuGa causes Ga vacancies in the GaAs substrate, which generates free electrons by the incorporation of Ge into the Ga vacancies. This reaction increases carrier concentration in the n^+-GaAs layer. As shown in above formula, the increase of carrier concentration(N_D^+), the reduction of contact resistance.

Therefore, the wide-process window of the hybrid ohmic contacts is attributed to the nonspiking Pd/Ge ohmic contact at low annealing temperature (~300℃) and also production of an alloyed AuGe contact at high annealing temperature (~400℃), resulting in hybrid ohmic contacts.

Ⅳ. CONCLUSIONS

We have developed thermally stable, low-resistance hybrid Pd/Ge/Ti/Au ohmic contact with good uniformity to the high-low doped n-type GaAs. The lowest contact resistivity of $3.0 \times 10^{-6}\ \Omega cm^2$ in a wide processing window, which was two times lower than that of Pd/Ge contact. The XRD, AES depth profile, and XTEM results showed that the good Pd/Ge/Ti/Au ohmic contact was due to formation of AuGa. The AuGa compound enhanced creation of more Ga vacancies, followed by incorporation of Ge into the Ga vacancies. This reaction increased carrier concentration at the GaAs/metal interface, followed by reduction of contact resistivity. In addition, formation of AuGa through fast indiffusion of Au toward GaAs substrate allowed the contact to be formed directly on the buried high-doped GaAs layer, which eliminated the resistance due to low-doped GaAs layer and the high-low resistance, with resulting further reduction of contact resistivity.

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