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A Study on the Reactor Protection System Composed of ASICs

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ABSTRACT

The potential value of the Application Specific Integrated Circuits(ASIC's) in safety systems of Nuclear Power Plants(NPP's) is being increasingly recognized because they are essentially hardwired circuitry on a chip, the reliability of the system can be proved more easily than that of software based systems which is difficult in point of software V&V(Verification and Validation). There are two types of ASIC, one is a full customized type, the other is a half customized type. PLD(Programmable Logic Device) used in this paper is a half customized ASIC which is a device consisting of blocks of logic connected with programmable interconnections that are customized in the package by end users. This paper describes the RPS(Reactor Protection System) composed of ASICs which provides emergency shutdown of the reactor to protect the core and the pressure boundary of RCS(Reactor Coolant System) in NPP's. The RPS is largely composed of five logic blocks, each of them was implemented in one PLD, as the followings. A). Bistable Logic B). Matrix Logic C).Initiation Logic D). MMI(Man Machine Interface) Logic E). Test Logic.

I. INTRODUCTION

The Reactor Protection System(RPS) in NPP's provides emergency shutdown of the reactor to protect the core and the reactor coolant system pressure boundary in nuclear power plants(NPP's). The most important thing in nuclear safety systems is to maintain the reliability of the system during the life of the plant. The RPS of Westinghouse type using solid state components such as transistors and TTL(Transistor Transistor Logic) ICs(Integrated Circuit's) or that of ABB-CE type using analog components such as relays uses many components in the board or panel, which has a possibility of decreasing the reliability of the system and increasing the difficulties on testability and maintainability of the system. So, the potential value of the Application Specific Integrated Circuits(ASIC's) in safety systems of Nuclear Power

Plants(NPP's) is being increasingly recognized because they are essentially hardwired circuitry on the chip which can integrate a large amount of electrical circuit in a small area, reliability could be improved as the result of reducing the number of components in the board or panel. There are two types of ASIC, one is a full customized type, and the other is a half customized type. The half customized one such as PLD is a device consisting of blocks of logic connected with programmable interconnections that are customized in the package by end users. That is more beneficial in cost and turn-around time from design completion to delivery of the ASIC than the full customized one which requires all processes of IC manufacturing. The PLDs used in this paper are Very Large Scale Integration(VLSI) ICs which could implement many components in one chip, which will enhance the reliability, testability and maintainability as the result of the reduction of the number of components used. The software based systems can overcome some weakness in hardware systems, but it introduces new uncertainty, which is S/W V&V. The software may be complex and has a possibility of having errors, but its reliability can not be proven by probabilistic means. To get the full potential of digital systems, error free S/W must be assured. The reliability check of software is very difficult to prove software reliability by testing, but PLDs are circuits connected by "hardwires" on a chip, their reliability can be established with more confidence by testing

II. SYSTEM DESCRIPTION OF THE CURRENT RPS

The RPS in YGN 3&4 NPPs is composed of separated four channels (A,B,C,D), and designed in negative logic circuits. For each trip function, there is a measurement channel, bistable logic, logic matrix and initiation circuit. The current signals of process variables measured in instruments are converted to voltage signals. These signals are brought to the voltage comparators and compared with the fixed or variable setpoints. If the input signals reach to the setpoints, the output relays of voltage comparators will become deenergized. The bistable trip will be determined by deenergization of output relays, to implement two out of four coincidence logic using contacts of four output relays, six matrix circuits are composed (AB, AC, AD, BC, BD, CD). The output contacts of six matrix circuits are serially connected to the initiation circuits. The initiation relays are used to open the contacts of RTSG(Reactor Trip Switch Gear) for tripping the reactor.

III. NEW SYSTEM DESIGN

1. Conceptual Design

The simplified configuration of the new RPS is like this, which has three logic blocks such as A/D(Analog to Digital), compare/coincidence, and test. The A/D block is for digitalizing analog input signals, the comp./coin. Block is for comparing them with setpoints and voting for the trip, and the test block is for checking the integrity of the path from input to output and logic blocks. In the protection systems, usually there are three types of setpoints, fixed, directional variable and rate variable.

2. Detailed Design

The RPS in NPP is composed of four channels(A,B,C,D), within each channel, bistable function and two out of four coincidence logic are included. The detailed configuration of the RPS using PLDs is shown as fig.1, and there are five PLDs such as bistable, matrix, initiation, MMI(Man Machine Interface) and test. All circuits in the PLD are designed in positive logic. This design is for 15 input analog signals, and all setpoints are considered to be fixed. The main features of each PLD are as the followings.

A. Bistable PLD

This logic is to compare the setpoints with the inputs which were converted in digital values from analog input values by Analog to Digital Converter(ADC). If any signal out of 15 input signals exceed the corresponding setpoint, the output of this PLD will generate logically true(one) value. The main features of this PLD are as the followings.

-. Control of multiplexor with 16 input signals (15 inputs : sensor inputs preconditioned, 1 input : test input)
-. Control of Sample/Hold(S/H) circuit with the input range of 10 volts
-. Control of ADC with 12 bit resolution
-. Comparator circuit which is for comparing the digitalized inputs with the setpoints
-. Hysteresis circuit which is for calculating the real setpoints in case of pre-trip or trip conditions through adder/subtractor circuits.
-. Signal interface with BBRAM(Battery Backup RAM), ADC, MMI PLD, and matrix PLD.
-. Self diagnostic test result signals to test PLD

B. Matrix PLD

The purpose of matrix logic is to check the coincidence between two channels, and there are six matrix combinations such as AB, BC, BD, CD, AC, AD channels from four channels. The main features of this PLD are as the followings.
-. Six matrix PLDs in the system
-. Power separation to meet IEEE Std 384-1981,"Standard Criteria for Safety Systems for Nuclear Power Generating Stations".
-. And and Or digital circuits to detect the coincidence between two channels
-. Self diagnostic test result signals to test PLD.

C. Initiation PLD

This PLD includes the final initiation circuit , time delay circuit and test circuit for itself. The main features of this PLD are as the followings.

-. Time delay is to block the test output signals, and only passes the actual actuation output signals, the previous outputs of time delays are feedback to the test PLD to check whether the integrity of the channel is good or not.

-. All outputs from six matrix PLDs are logically Ored to actuate trip signals.

-. Self diagnostic test result signals to test PLD

D. MMI(Man Machine Interface) PLD

The alarm status will be indicated in alarm sound, and lamps. The setpoint values will be displayed in seven segment LEDs. The main features of this PLD are as the followings.

-. Max/Min display of the last values

-. Display of the current value

-. Display of setpoint value

-. The setpoints are adjusted by thumb wheel switches

-. Self diagnostic test result signals to test PLD

E. Test PLD

The RPS is a safety system, so its reliability is important. TO check its integrity, each channel is periodically tested by the test PLD, there are two testing methods, one is the on-line test, and the other is the manual test, in later case the corresponding one channel is bypassed, the remaining channels should satisfy two out of three coincidence logic for the trip of the plant. The main features of this PLD are as the followings.

-. The test sequence is begun with the channel A test.

-. All other PLDs's internal test results will be input to the test PLD, and the results will be displayed in the indicators.

-. The internal test result of the PLD will also be indicated.

-. There is a Digital to Analog Converter(DAC) in each test module which can trip the RPS.

-. Test PLD initiate the test and receives the results from other PLDs in the same channel.

-. After the test of local PLDs in the channel, it will initiate the start of the overall channel test.

-. There is one test input point which is connected to the one input of multiplexor. Its input is controlled by the DAC with the range of 10 volts of test module, the output of DAC is controlled by test PLD.

-. During the test of bistable PLD in the manual test, MUX, ADC and RAMs are tested separately.

-. The initiation logic which is composed of six AND gates serially connected, the corresponding matrix logic is bypassed.

-. The DAC input value is above the setpoint, the input pulse is a short pulse, its test is performed by test PLD, and input control voltages of DAC and test input form the other channel is a one shot positive pulse with a finite time pulse width, but its time is less than the time delay, so it will not actuate the real trip, in this case, the input signal form the other channel is inhibited, and the tripped test input is enabled.

-. If the manual test is required, it is also possible.

-. The timer synchronizes the ADC and self test features.

IV. CONCLUSION

The simulation result is shown as Fig.2. The ASIC is essentially hardwired circuitry on a chip, reliability can be proved more easily than with software based systems which requires software verification and validation(S/W V&V). PLDs which are one type of ASIC are devices consisting of logic blocks connected with programmable interconnections that are customized in the package by end users. Uncertainties about the reliability of software based systems in nuclear applications has proved costly, with a negative impact on the upgrade cost/benefit analysis. The reliability check of software is very difficult to prove software reliability by testing. This hardwired circuit built in PLDs will increase the reliability of the system.

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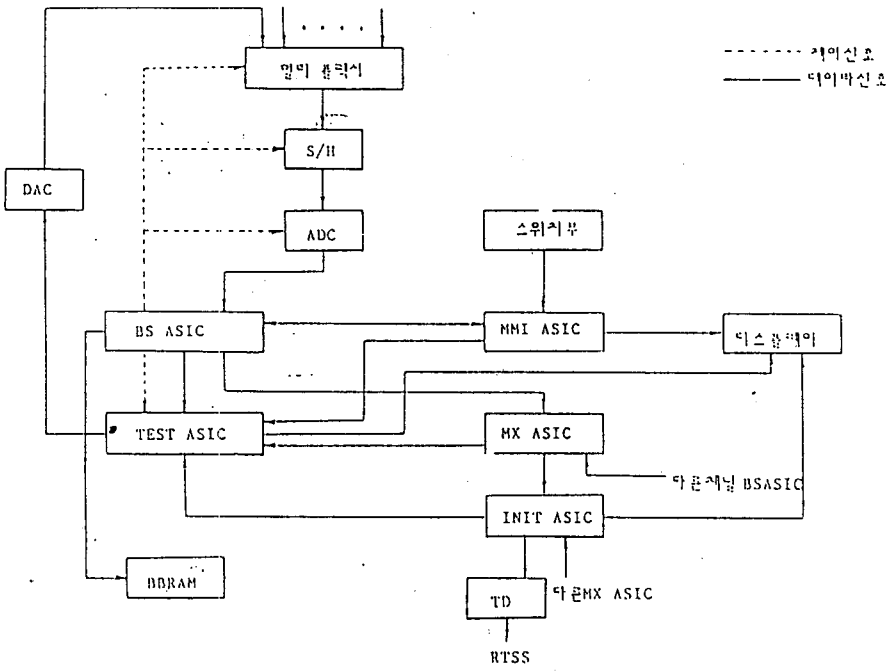

Fig.1. The one channel of RPS composed of ASICs

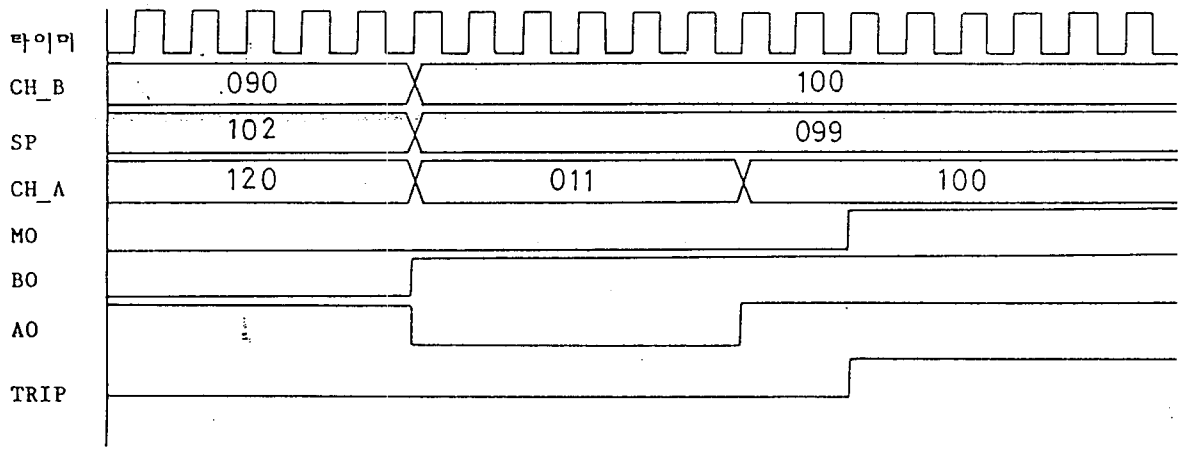

Fig.2. Simulation Result