Low-Temperature Si and SiGe Epitaxial Growth by Ultrahigh Vacuum Electron Cyclotron Resonance Chemical Vapor Deposition (UHV-ECRCVD)

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Low-temperature epitaxial growth of Si and SiGe layers on Si is one of the important processes for the fabrication of the high-speed Si-based heterostructure devices such as heterojunction bipolar transistors. Low-temperature growth ensures the abrupt compositional and doping concentration profiles for future novel devices. Especially in SiGe epitaxy, low-temperature growth is a prerequisite for two-dimensional growth mode for the growth of thin, uniform layers. UHV-ECRCVD is a new growth technique for Si and SiGe epilayers and it is possible to grow epilayers at even lower temperatures than conventional CVD's. SiH_4 and GeH_4 and dopant gases are dissociated by an ECR plasma in an ultrahigh vacuum growth chamber. *In situ* hydrogen plasma cleaning of the Si native oxide before the epitaxial growth is successfully developed in UHV-ECRCVD.

Structural quality of the epilayers are examined by reflection high energy electron diffraction, transmission electron microscopy, Nomarski microscope and atomic force microscope. Device-quality Si and SiGe epilayers are successfully grown at temperatures lower than 600 °C after proper optimization of process parameters such as temperature, total pressure, partial pressures of input gases, plasma power, and substrate dc bias. Dopant incorporation and activation for B in Si and SiGe are studied by secondary ion mass spectrometry and spreading resistance profilometry. Silicon p-n homojunction diodes are fabricated from *in situ* doped Si layers. I-V characteristics of the diodes shows that the ideality factor is 1.2, implying that the low-temperature silicon epilayers grown by UHV-ECRCVD is truly of device-quality.

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Outline

- Introduction
  - Low temperature Si & SiGe epitaxy
  - In situ hydrogen plasma cleaning
- Si & SiGe epitaxy by UHV-ECRCVD
  - process parameters
  - growth kinetics
  - defect morphology
  - critical thickness
  - in situ doping
- Fabrication of a Si pn junction diode
  - fabrication procedure
  - I-V characteristics
- Conclusions

Motivation

- **Abrupt Compositional & Doping Profiles**
  - Reduced Thermal Diffusion
  - Reduced Autodoping
- **Reduction of Thermally-Induced Defects**
- **Especially in Si/SiGe Heteroepitaxy**
  - Layer-by-Layer Growth
  - Strained Layer
- **Fabrication of Novel Devices**
  - HBT, HEMT, RTD, Optoelectronic Devices, etc.

SiGe/Si Heterojunction Bipolar Transistor (HBT)

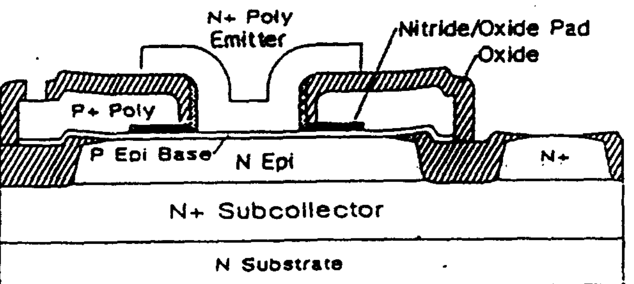


Fig. 1. Schematic cross section of the non-self-aligned bipolar structure with an epitaxial base.

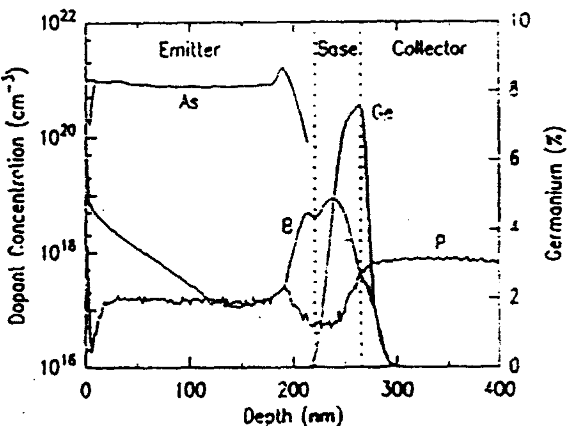
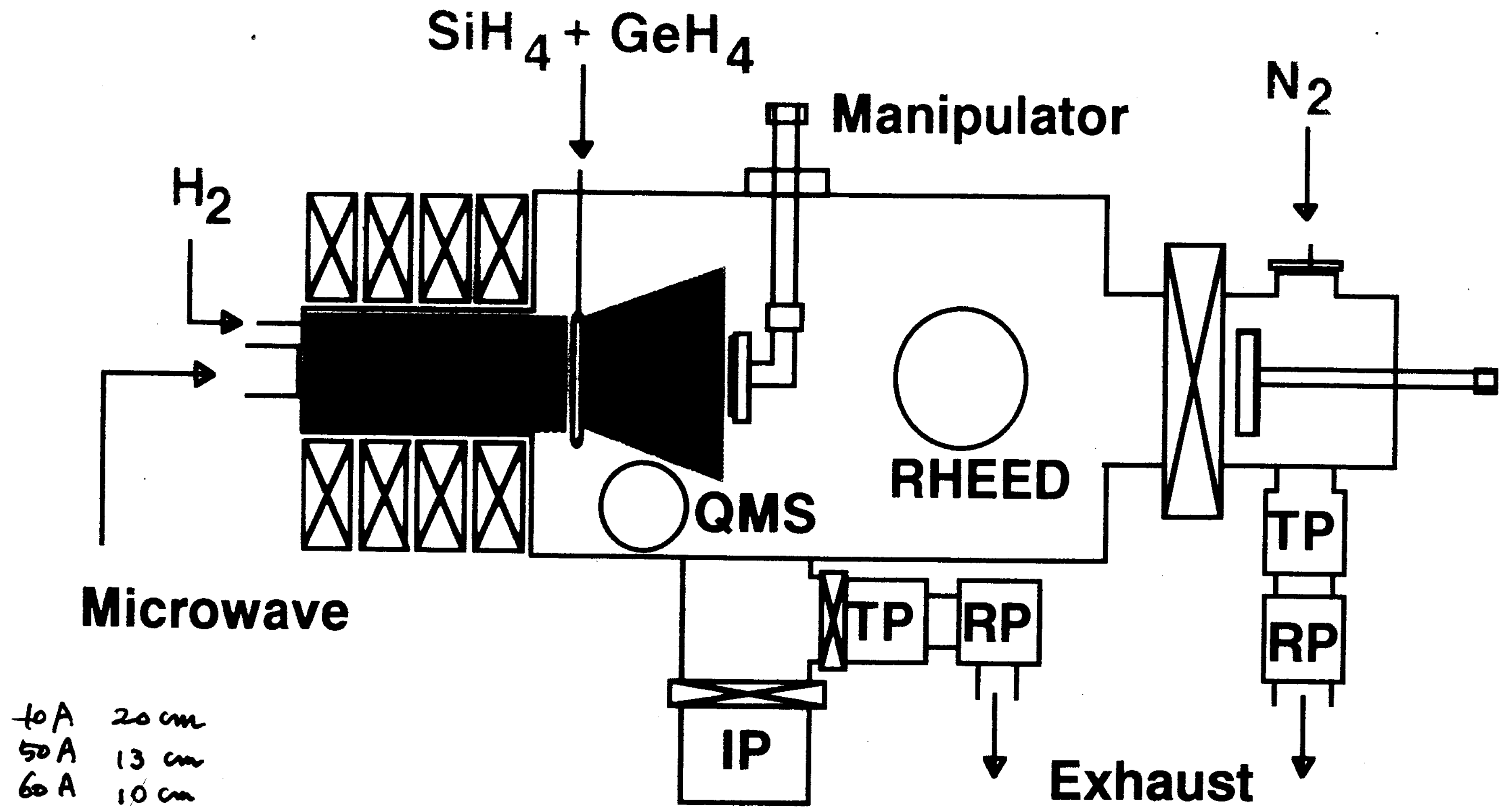


Fig. 2. SIMS profile of a completed SiGe-base device. A base width of 45 nm was achieved.

G.L. Patton, J.H. Comfort, B.S. Meyerson, E. Crabbe, G.J. Scilla
E.D. Fresart, J.M.C. Stork, J.Y.-C. Sun, D.L. Harame, and J.N. Burghartz,
IEEE Electron Device Lett. 11, 171(1990)

EY/ISRC/SNU

UHV-ECRCVD System



Effect of the Substrate DC Bias on *in situ* Hygrogen Plasma Cleaning

Surface Cleaning Condition:

Substrate Temperature : 560 °C
Plasma Power : 100 W
Bobbin Current : 50 A
H_2 Flow Rate : 74 sccm
Exposure Time : 2 min

RHEED

XTEM

c

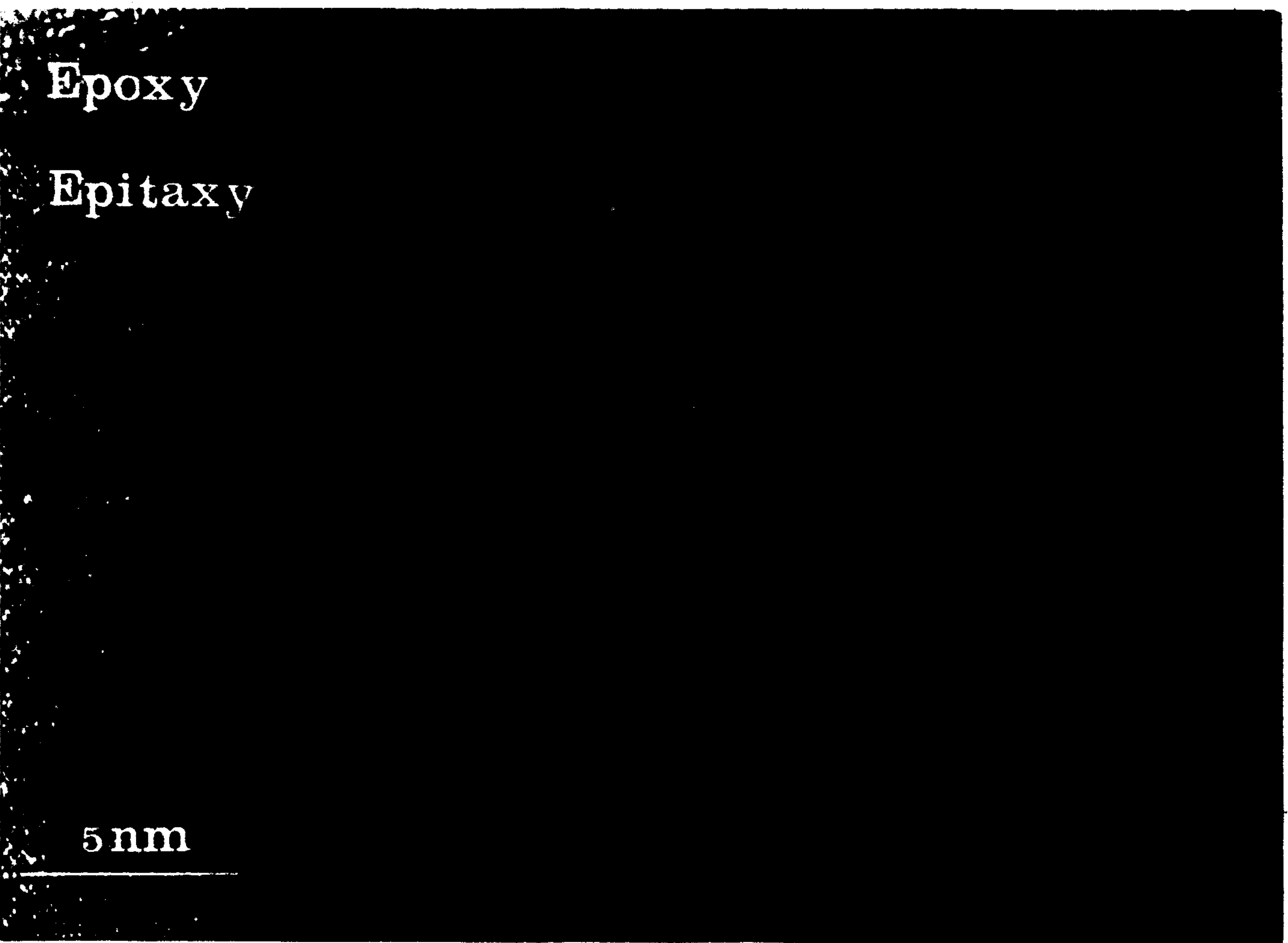
d

100 nm

floating | + 10 V

High Resolution TEM of Defective Si Epilayer

HRTEM of Dislocation-free Si Epilayer by UHV-ECRCVD



SiGe Heteroepitaxy by UHV-ECRCVD

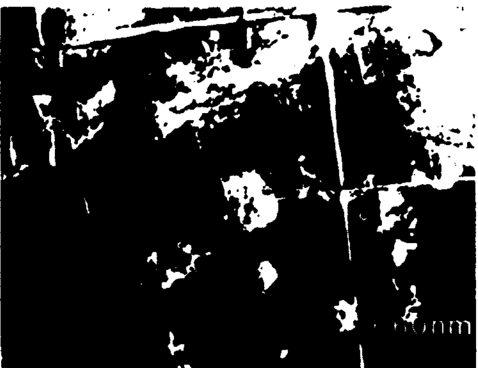
- ***In situ* hydrogen plasma cleaning**
  - process parameters: temperature, substrate DC bias, magnet current, plasma power, total pressure, etc.
  - defect formation : ion flux and exposure time
  - RHEED, TEM, dilute Schimmel etching, AFM

- **Plasma deposition**
  - based on Si homoepitaxy condition:
    440 °C, +100 V, 40 A, 50 W, 4 mTorr
  - source gases: SiH_4, GeH_4, H_2, B_2H_6
  - process parameters: temperature, substrate DC bias, magnet current, plasma power, total pressure, GeH_4/SiH_4

- **Characterization**
  - tools: TEM, RBS, SIMS, PL, Lifetime Measurement
  - crystallinity
  - growth kinetics
  - critical thickness
  - dopant incorporation

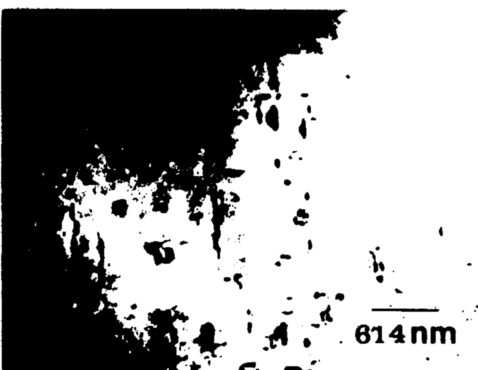
Change of defect morphology with growth parameters

(a) +100V, 50W, 40A, 22%, 410 Å



(b) +10V, 50W, 40A, 21%, 1994 Å

(c) +100V, 100W, 40A, 31%, 520 Å



(d) +100V, 50W, 45A, 31%, 1353 Å

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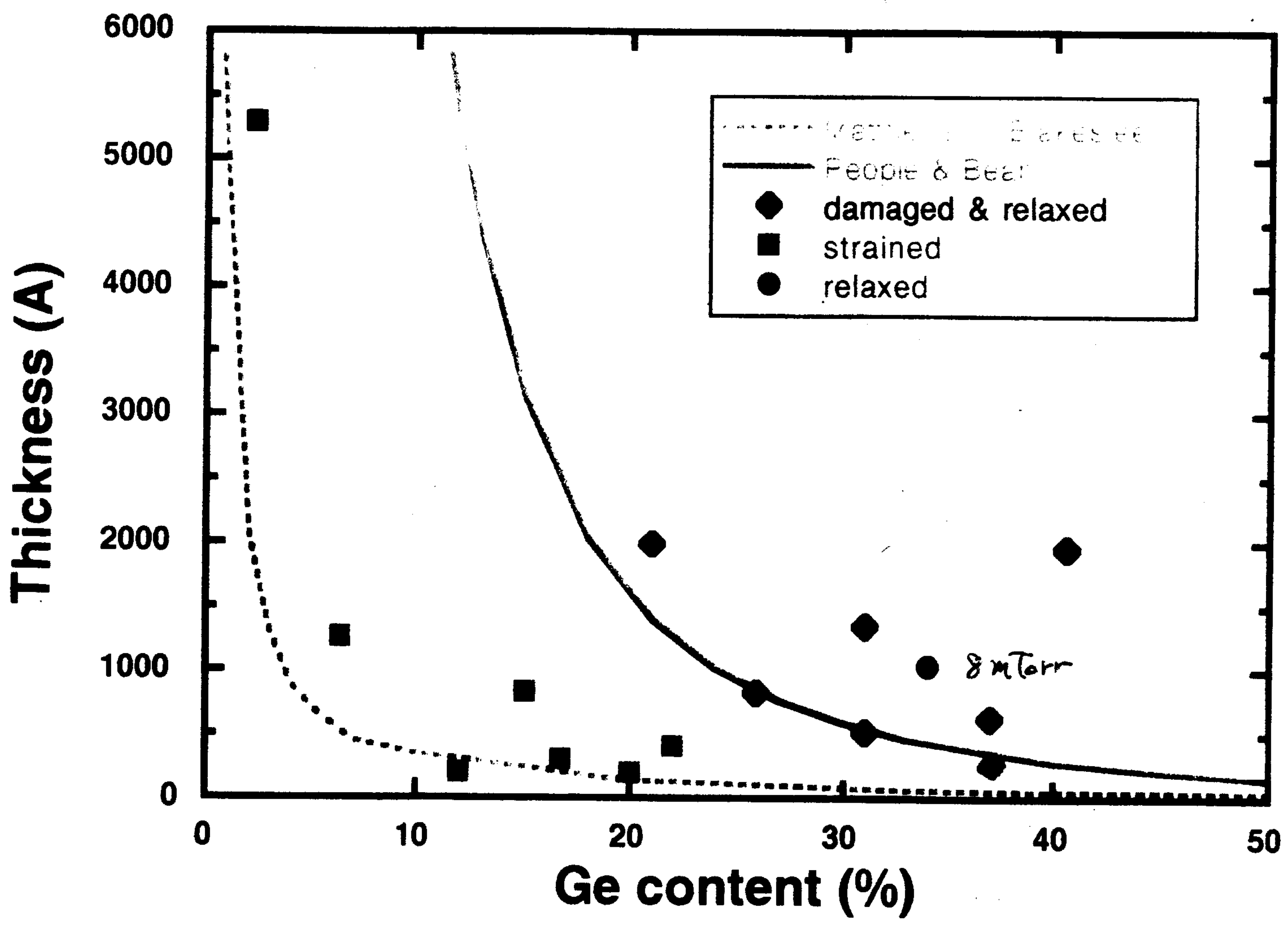

Critical Thickness
Thickness (A)
Ge content (%)
6000
5000
4000
3000
2000
1000
0
0
10
20
30
40
50
damaged & relaxed
strained
relaxed
8 mTorr

XTEM Image of a Multilayer Structure

- 440°C, 10mTorr
- 5 periods

Si / $Si_{0.9}Ge_{0.1}$
5 period
Si : 700Å
SiGe : 400Å

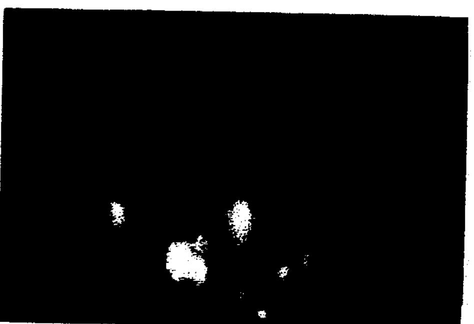
Experiment

Effect of Process Parameters on *in-situ* B-doped Layer Crystallinity

Result

Effect of Temperatures on *in-situ* B-doped Epi-layer Crystallinity

P_T= 8mTorr, I_m= 40A, microwave power= 50W
H_2= 74sccm, SiH_4= 1sccm, B_2H_6/H_2= 9sccm



440°C

470°C

Result

Effect of Microwave Power on *in-situ* B-doped Epi-layer Crystallinity

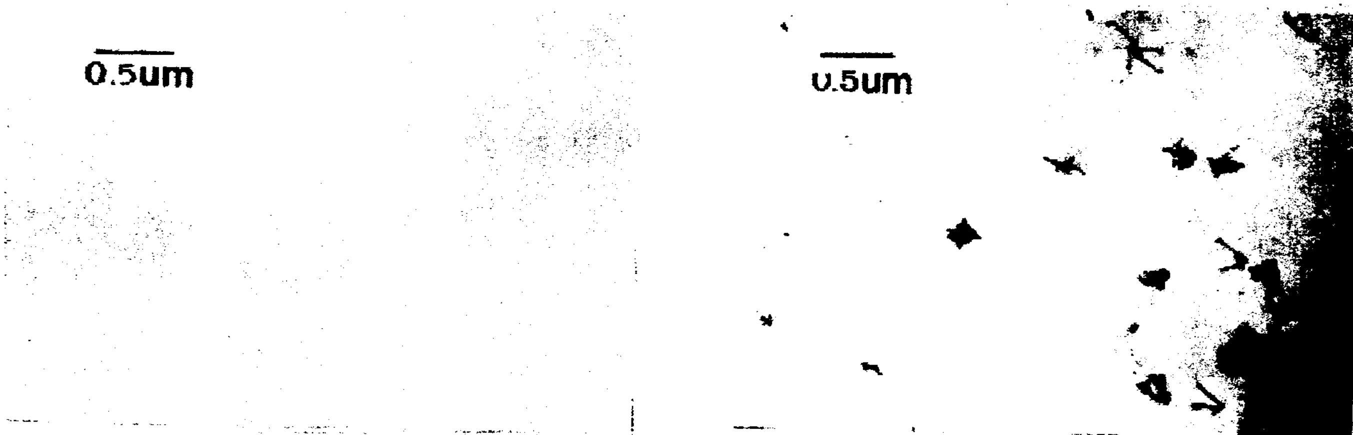
P_T= 8mTorr, I_m= 40A, T_d= 470°C
H_2= 74sccm, SiH_4= 1sccm, B_2H_6/H_2= 1 ~ 9sccm

50W

100W

Effect of Substrate DC Bias on *in-situ* B-doped Epi-layer Crystallinity

P_T= 8mTorr, I_m= 40A, T_d= 510°C, Power= 50W
H_2= 74sccm, SiH_4= 2sccm, B_2H_6/H_2= 14sccm



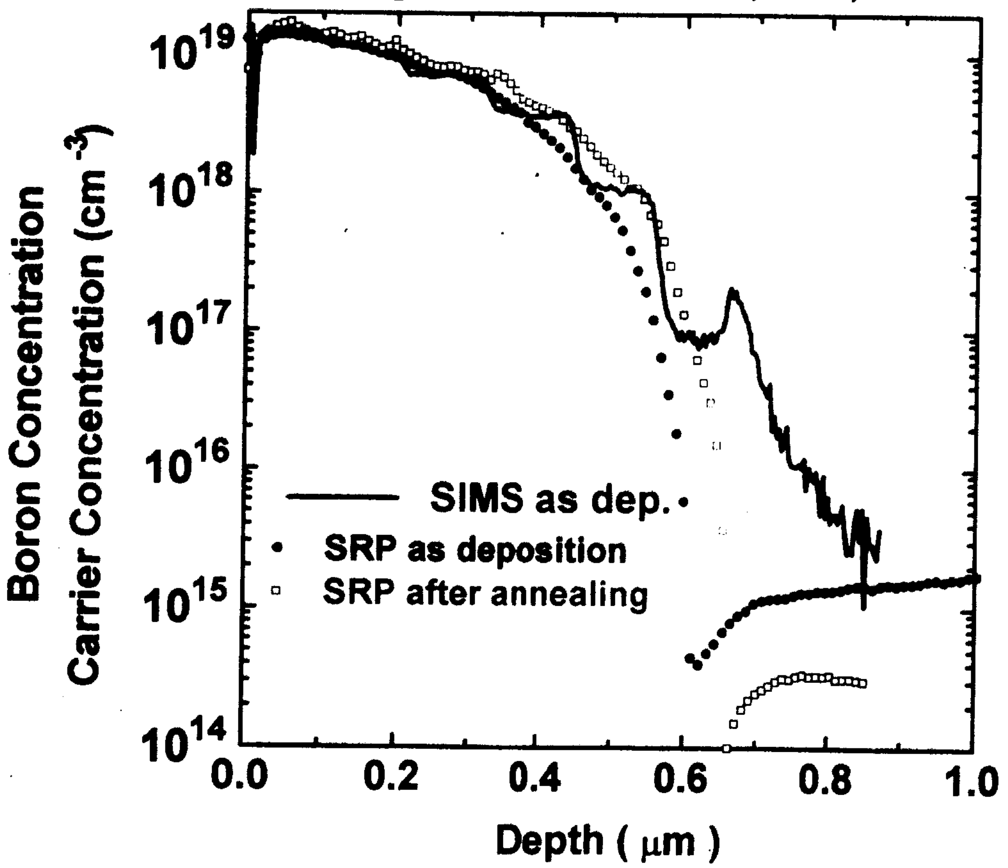
+30V +100V

Electrical Properties of in-situ B-doped Epi-layer

SIMS Depth Profile of *in-situ* B-doped Epi-layer and Electrical Activation of Boron by Annealing

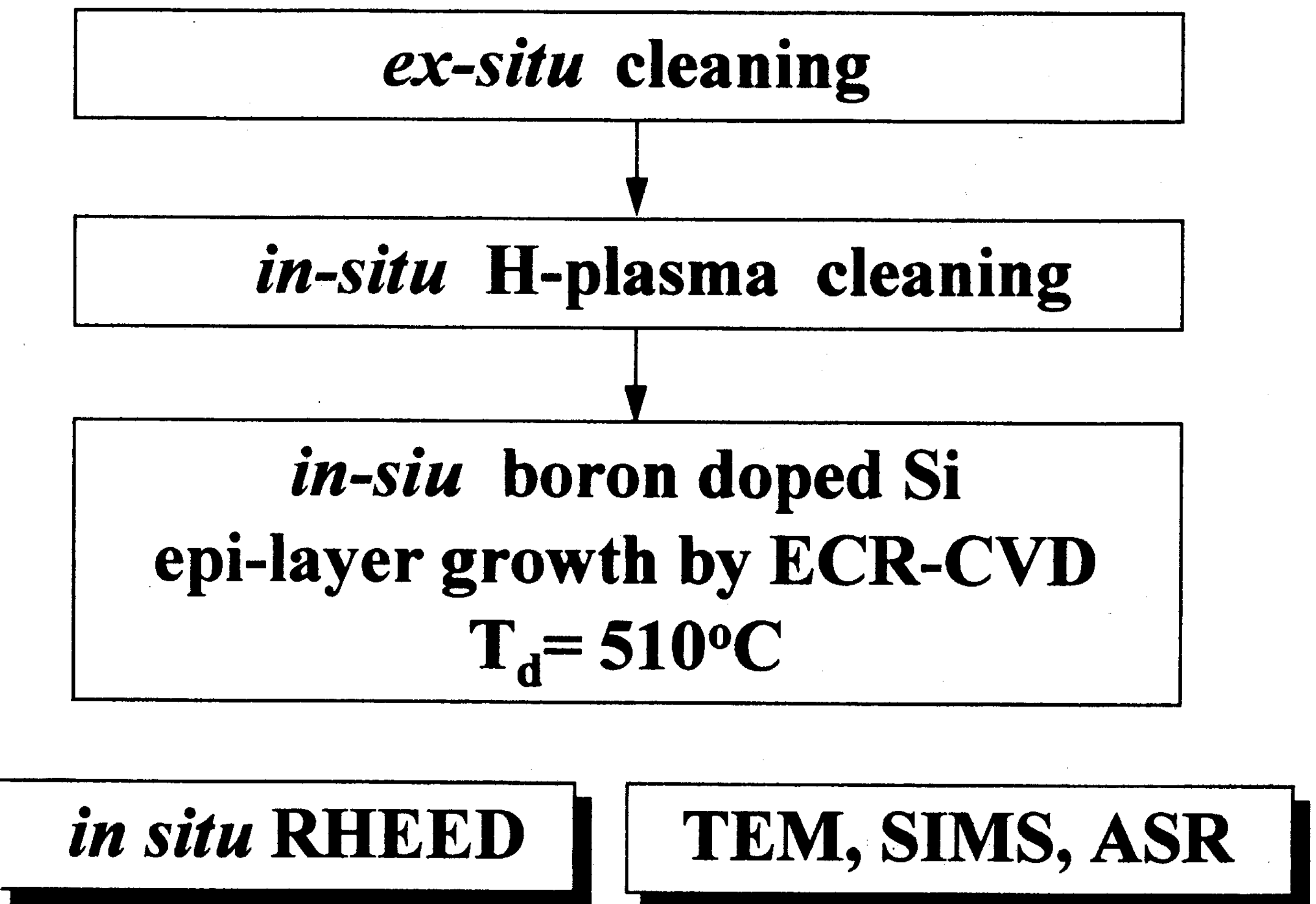
510°C, 50W, 40A, +30V, SiH_4=2sccm, B_2H_6/H_2= 0-18 sccm

Annealing conditions : 600°C, 2hrs, vacuum



Experiment

Experimental Procedure



in situ RHEED

TEM, SIMS, ASR

Experiment

Fabrication Process of p^+n^+ Mesa Diode

n^+ buried layer (As, 80 keV, $1x10^{15}/cm^2$)

$1x10^{18}/cm^3$ B-doped Si epi-growth

As dep. and annealing (600°C, 2 hrs, vacuum)

$1x10^{19}/cm^3$ B-doped Si epi-growth

Mesa etching (Cl_2 + He)

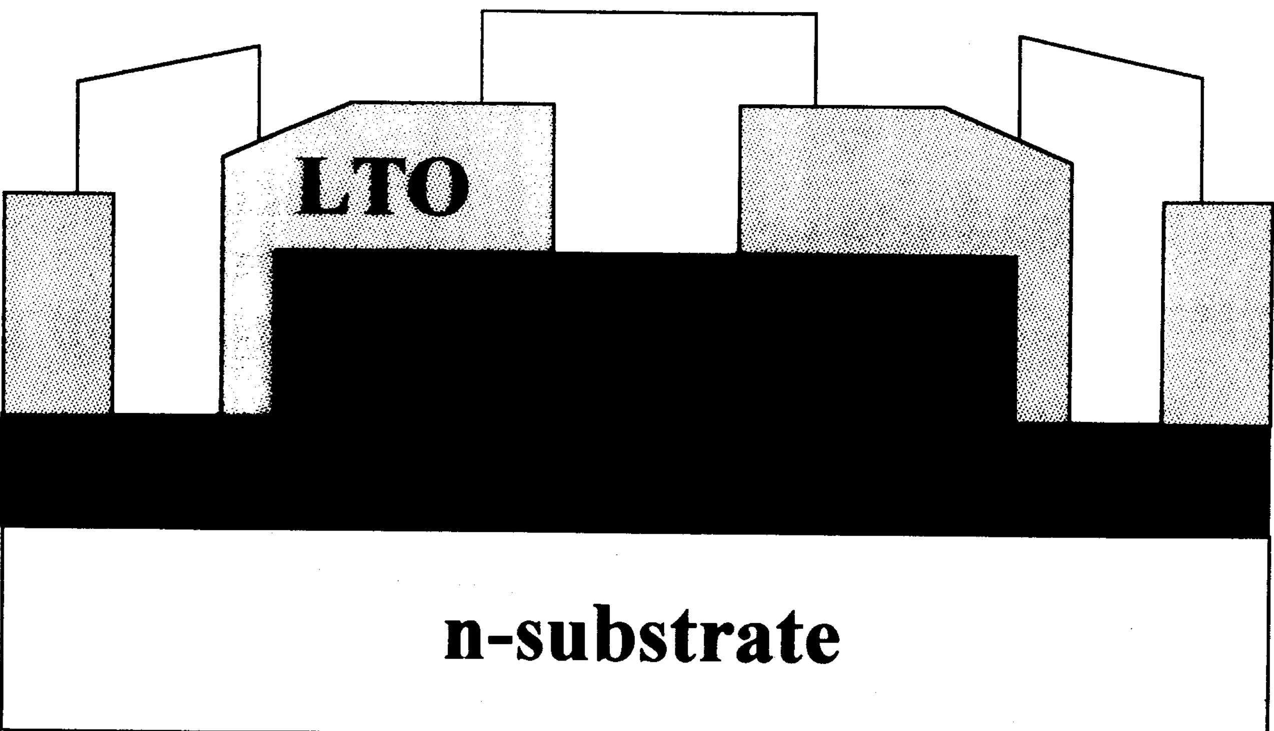
LTO deposition (PECVD TEOS)

1%-Si Al sputter deposition

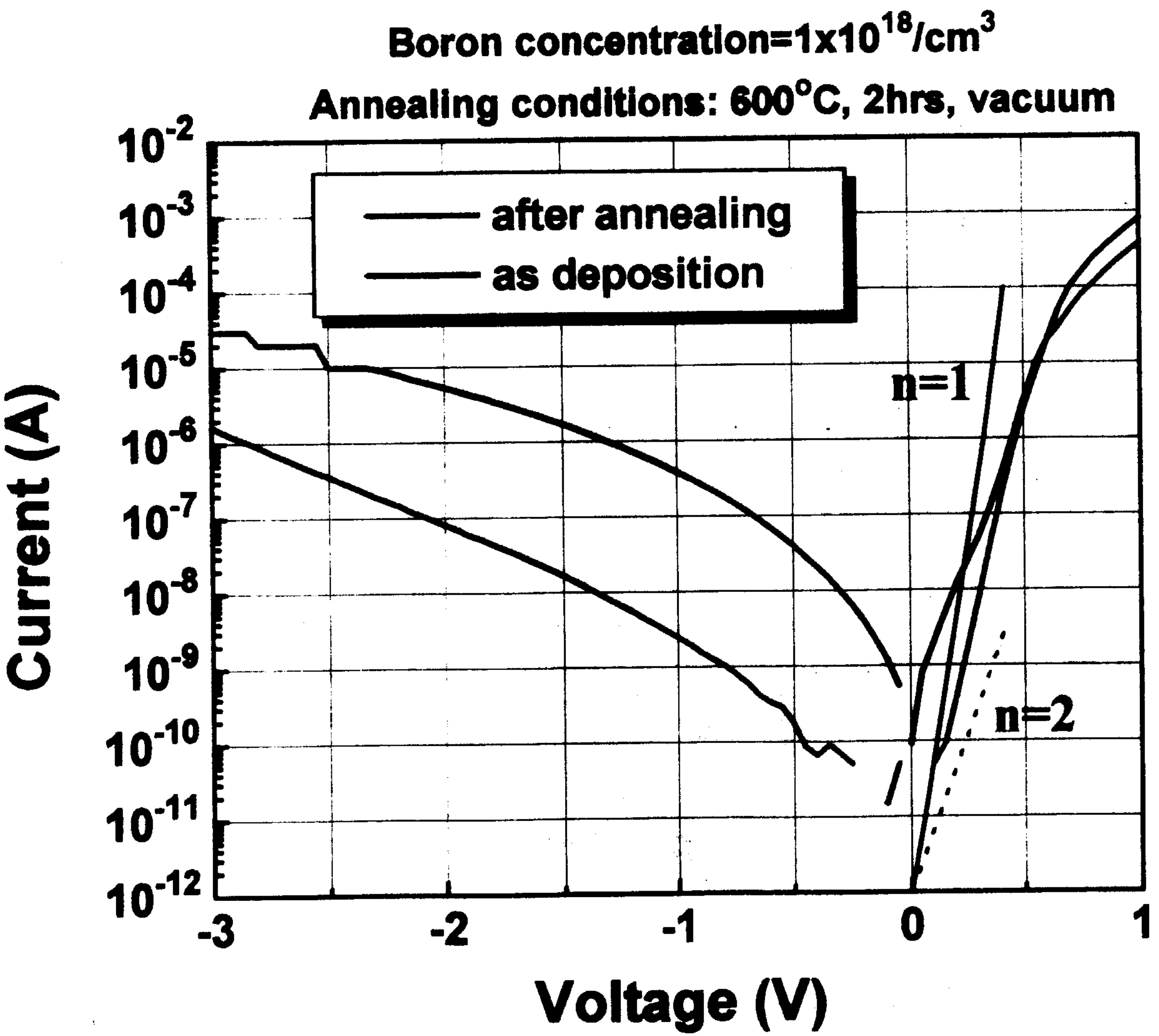
Alloy (450°C, FG, 30 min)

Structure of p^+n^+ Mesa Diode

L/W = 1.5/20 μm



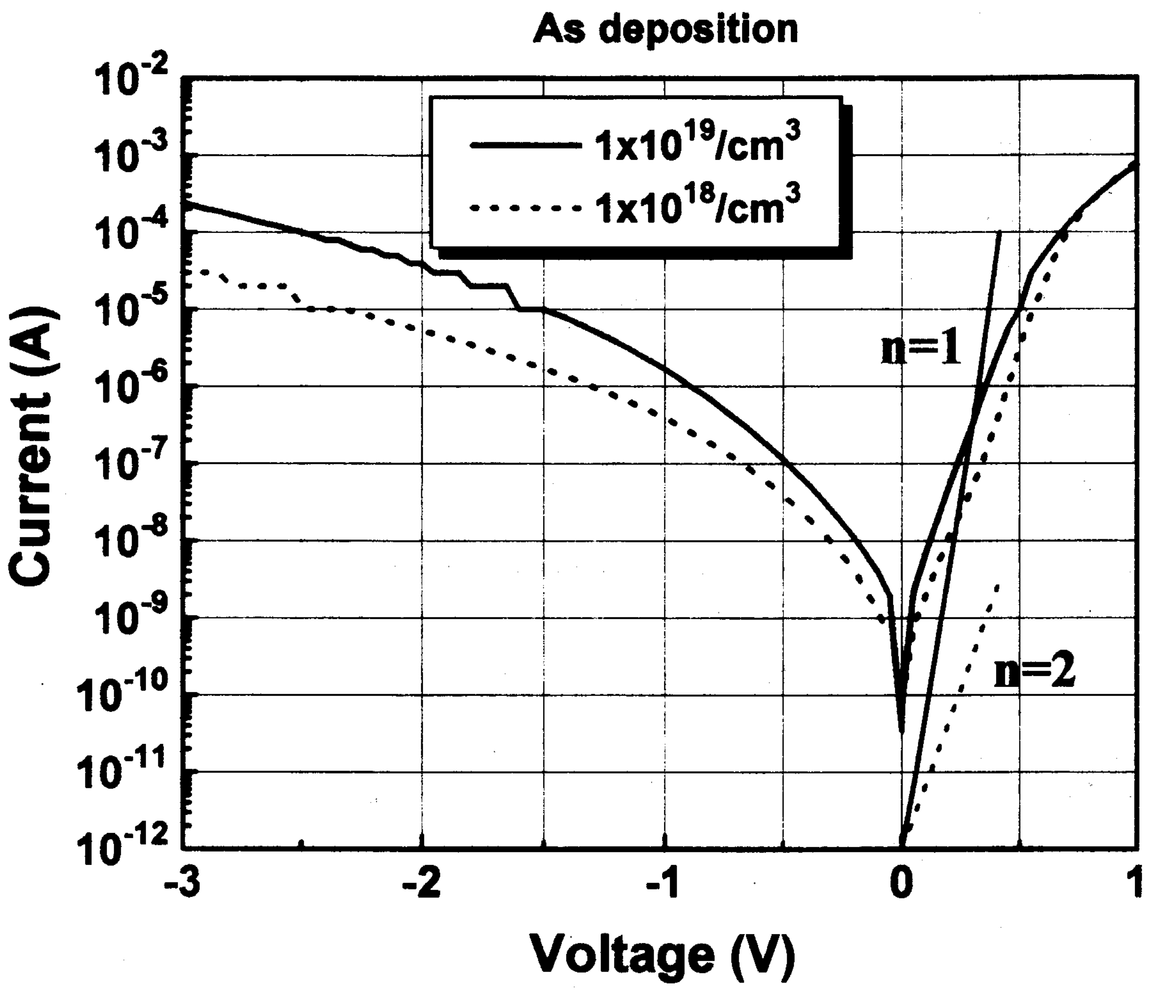
Effect of Annealing on I-V Characteristics of p^+n^+ Diodes



Ideality factor n

$$I = I_0(e^{qV/nkT}-1)$$

Effect of Doping Conc. on I-V Characteristics of p^+n^+ Diodes



Ideality factor (n)

$I = I_0 \left(\exp\left(\frac{qV}{nkT}\right) - 1 \right)$

n = 1 : diffusion controlled

n = 2 : recombination controlled / generation

Conclusions

- Device-quality Si and SiGe epitaxial layers can be grown by UHV-ECRCVD with proper optimization of process parameters.
- In situ doping of B and As were studied, and it is possible to dope Si up to $1x10^{19}$/cc without defect generation.
- A Si pn junction diode was fabricated with the plasma-grown Si layers, and the ideality factor was 1.2.
- UHV-ECRCVD is a promising growth technique for the low-temperature, novel device fabrication.