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Analysis of Inverter with Switched Snubber Using N-channel MOS-FET

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Abstract This paper describes the analysis of the operation of the switched snubber in order to depress the surge voltage in the MOS-FET inverter. In this paper, the N-channel MOS-FET which operates faster than the P-channel MOS-FET was used for the inverter circuit. So, the inverter and switched snubber can operate at high-frequency in the order of MHz. The cause of generating the surge voltage in the high frequency inverter has been cleared, and then how to depress the surge voltage using the switched snubber consisting of an N-channel MOS-FET has been given. Furthermore, described is the power loss within the switched snubber which is made of an N-channel MOS-FET. The inverter having the N-channel MOS-FET used as a switched snubber can drive such a low impedance load such as mega-sonic transducer for a mega-sonic studied cleaner sufficiently.

Keywords Inverter, Snubber, Switched snubber

1. Introduction

When semiconductor wafers, LCD substrates or other industrial materials are washed by the megasonic cleaning, materials are not damaged even if the cavitation has occurred[1]. The ultrasonic transducer used for the cleaning is a very thin device so that the transducer exhibits low impedance at the resonance frequency[2]. In order to clean materials powerfully at high frequency, the power capacitance of the ultrasonic transducer is made high in many cases. In this case, the size of the ultrasonic transducer is large, or ultrasonic transducers of small size are connected in parallel. So, the impedance of the ultrasonic transducer gets smaller than normal use. Therefore, the impedance of the ultrasonic transducer which operates at high power, at high frequency in the order of MHz goes low[3]. When the load which has low impedance is operated by the switching type inverter at high frequency, at high power, the surge voltage may be generated across the switching elements. The surge voltage sometimes destroys the circuit. Therefore, many kinds of snubbers are used in order to depress the surge voltage. The switched snubber circuit which consists of a switching element and a capacitor connected in series has smaller loss than a CR snubber circuit and can depress the surge voltage satisfactorily[4]-[5]. So, the switched snubber constructed using a P-channel MOS-FET has been reported. However, P-channel MOS-FET operates slower than N-channel MOS-FET so that it cannot operate at high frequency of MHz. So, a set of N-channel MOS-FET's are used as a main switching element and switched snubber so that the inverter is constructed. This circuit can drive the ultrasonic transducer sufficiently, and the switched snubber can depress the surge voltage.

This paper describes the cause of generating the surge voltage in the high frequency inverter, and then how to depress the surge voltage using the switched snubber using N-channel MOS-FET. Furthermore, described is the current flowing through the switched snubber which of the N-channel MOS-FET

2. Cause of the Surge Voltage

At first, the basic inverter circuit configuration is given as an example. Figure 1 shows the basic inverter constructed using an N-channel MOS-FET as a switching element. In order to decrease the effective ON-resistance of the MOS-FETs and to increase the power capacitance, 5 MOS-FETs are connected in parallel. Therefore, the ON-resistance of MOS-FETs is one fifth of a single MOS-FET.

Figure 2 shows the equivalent circuit of the MOS-FET when the MOS-FET of the inverter turns off. E_{OFF} is voltage across the switching element when the switching element of the inverter are turned off. L_S is parasitic inductance including the

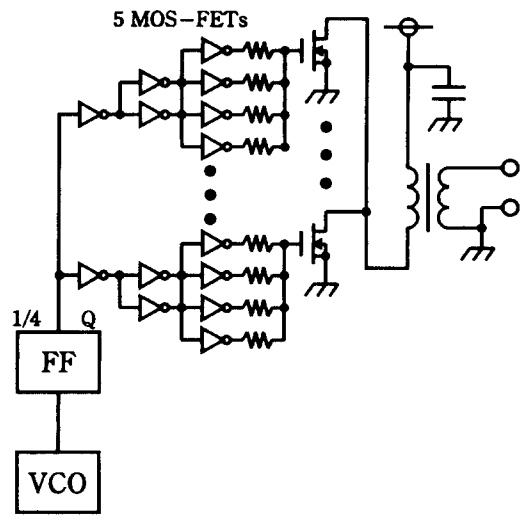


Figure 1. Basic inverter using N-channel MOS-FET.

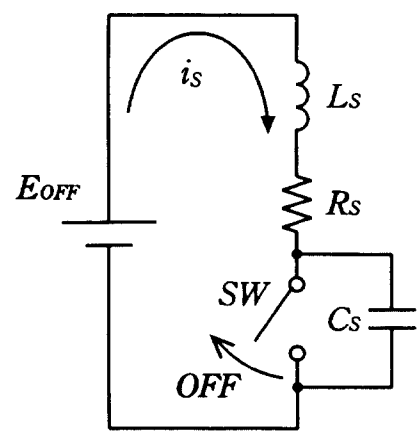


Figure 2. Equivalent circuit of MOS-FET.

leakage inductance of the output transformer. R_S is the parasitic resistance of the circuit wiring connections and load resistance looking from the primary winding on the output transformer into the load. SW is the switching element. C_S is the parasitic capacitance of the switching elements.

The OFF-resistance of the switching element is small because an MOS-FET is used as a switching element. Therefore, the OFF-resistance of the switching element is defined as infinity value and the OFF-resistance of the switching element is disregarded.

From Figure 2, differential equations are given by equations (1) and (2).

$$L_S \frac{di_S}{dt} + R_S i_S + v(t) = E_{OFF} \quad \cdots\cdots\cdots(1)$$

$$i_S = C_S \frac{dv(t)}{dt} \quad \cdots\cdots\cdots(2)$$

where, i_S is the current flowing through the drain circuit and v(t) is the voltage across the switching elements when the switching elements turn off.

From equations (1) and (2), the equation (3) is given.

$$C_S L_S \frac{d^2v(t)}{dt} + C_S R_S \frac{dv(t)}{dt} + v(t) = E_{OFF} \quad \cdots\cdots\cdots(3)$$

When the surge voltage is generated, the solution of a characteristic equation obtained from the equation (3) includes the imaginary part. Therefore, the requirement for generating the surge voltage is given by the equation (4)

$$\frac{4L_S}{C_S R_S} > 1 \quad \cdots\cdots\cdots(4)$$

In the equation (4), the imaginary part may be generated if,

(i) The parasitic inductance is of large value.

(ii) The parasitic capacitance of the switching elements is of a small value.

and,

(iii) The load resistance is of small value.

Therefore, when the ultrasonic transducer is used as an inverter load, the surge voltage can be generated easily.

At the time just before the switching elements turn off, no surge voltage is generated across the switching elements. At the time, the current flowing through the switching elements is defined as I_{ON} since the switching elements are kept turned on. The equations (5) and (6) can thus be obtained.

$$v(0) = 0 \quad \cdots\cdots\cdots(5)$$

$$i_S(0) = I_{ON} \quad \cdots\cdots\cdots(6)$$

Therefore, when the switching elements turn off, the surge voltage across the switching elements is given by the equation (7).

$$v(t) = E_{OFF}\left\{1 - \frac{\omega_o}{\omega_f} e^{-\sigma t} \sin(\omega_f t + \theta)\right\} + \frac{I_{ON}}{C_S \omega_f} e^{-\sigma t} \sin \omega_f t \quad \cdots\cdots\cdots(7)$$

where, the resonance angular frequency ω_0, attenuation constant σ, phase constant ω_f, phase angle θ are given by equations (8) through (11), respectively.

$$\omega_O = \frac{1}{\sqrt{C_S L_S}} \quad \cdots\cdots\cdots(8)$$

$$\sigma = \frac{R_S}{2L_S} \quad \cdots\cdots\cdots(9)$$

$$\omega_f^2 = \omega_O^2 - \sigma^2 \quad \cdots\cdots\cdots(10)$$

$$\theta = \tan^{-1} \frac{\omega_f}{\sigma} \quad \cdots\cdots\cdots(11)$$

When the switching elements are kept turned on, current I_{ON} flows through the parasitic inductance L_S, load resistance R_S, and switching elements SW so that the energy is moved to the parasitic inductance L_S. When the surge voltage can be generated, the energy moves from the inductance L_S to the parasitic capacitance C_S. Therefore, the surge voltage may be generated across the switching elements.

3. Effect of Depressing Surge Voltage

A. Switched snubber circuit

The surge voltage can be depressed by increasing the parasitic capacitance.

Figure 3 shows the circuit diagram of the inverter with a switched snubber. The switched snubber consists of an N-channel MOS-FET used as a switching element, and a capacitor. The N-channel MOS-FET operates faster than the P-channel MOS-FET. The operation of this snubber defers from the P-channel MOS-FET snubber. The switching elements and a capacitor are connected in series, and they are connected to the main switching elements in parallel. When the main switching elements are turning off, the switching element used as a snubber is kept turned on. This is the reason that the parasitic capacitance of the main switching elements can be increased. Therefore, the surge voltage across the main switching elements can be depressed.

B. Effect of switched snubber

Figure 4 shows the calculated and measured voltage waveforms across the main switching elements. Where, the parameters are given as R_S=5.5Ω, L_S=1.2×10²nH, and C_S=6.5×10²pF. These parameters are substituted into the equation (4),

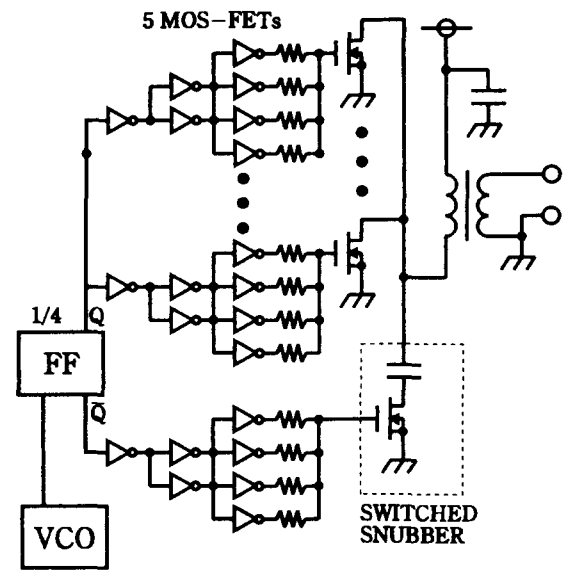
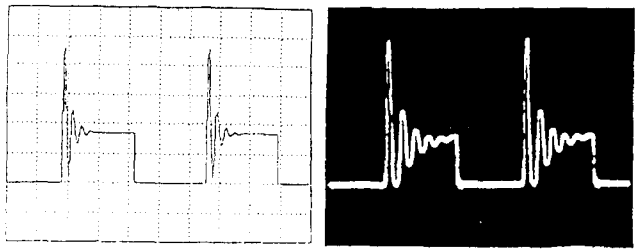
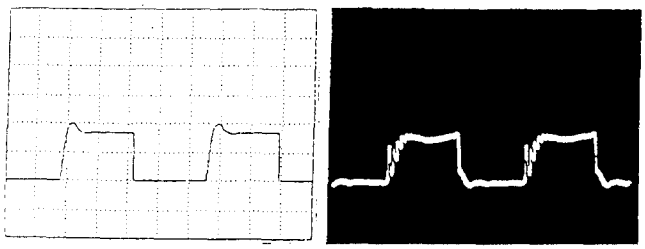


Figure 3. Circuit diagram of the inverter with a switched snubber.



(a) Calculated waveform. (b) Measured waveform.

Figure 4. Surge voltage waveforms.



(a) Calculated waveform. (b) Measured waveform.

Figure 5. Voltage waveforms appearing across the main switching elements with a switched snubber.

$$\frac{4L_S}{C_S R_S^2} = \frac{4\times 120\times 10^{-9}}{650\times 10^{-12}\times 5.5^2} = 24 >> 1 \qquad \cdots\cdots\cdots(12)$$

this equation meets the requirement of generating the surge voltage. Then, the surge voltage can be generated across the switching elements.

Figure 5 shows the calculated and measured voltage waveforms across the main switching elements when the switched snubber is connected to the inverter. Where, the capacitance of the switched snubber is given as C_{SS}=10000pF, and the other parameters are same as those of Figure 4. These parameters are substituted into the equation (4),

$$\frac{4L_S}{(C_S + C_{SS})R_S^2} = \frac{4\times 120\times 10^{-9}}{(10000+650)\times 10^{-12}\times 5.5^2} = 1.5 > 1 \qquad \cdots\cdots\cdots(13)$$

this value is not large enough to generate the surge voltage. Therefore, it can be seen that the surge voltage is depressed by the switched snubber circuit. From Figure 5, the switched snubber depresses the surge voltage sufficiently.

4. Power Loss of Switched Snubber

In Figure 5, when the main switching elements turn on, the drain-source voltage across the main switching elements cannot be changed quickly. This reason is that the charge stored within current charged in the capacitor of the switched snubber C_{SS} flows when the main switching elements turn on. That is, when the main switching elements turn on, the voltage across the switched snubber is increased up to the voltage which equal to the voltage across the main switching elements at the time just before the switching elements turn on. So, when the switching element of the switched snubber turns off, the PN junction between the drain and substrate of the N-channel MOS-FET used as the switching element is forward biased. Therefore, the charge in the capacitor flows through the PN junction between the drain and substrate and then through the main switching elements. The fall time is thus increased. In this case, the more the capacitance is increased, the more the current increases.

When the current flows through the switched snubber connected to the inverter, the loss power P_{SS} is given by the equation (14),

$$P_{SS} = \frac{1}{2} C_{SS} E_{DS}^2 f_O \qquad \cdots\cdots\cdots(14)$$

where f_O ($=\omega_O/2\pi$) is the operating frequency of the main switching elements, and E_{DS} is the voltage across the main switching elements just before they turn on.

Figure 6 shows the calculated and measured loss powers by the current flowing through the capacitor. In the calculation, f_O=1MHz, C_{SS}=4700pF are assumed. The measured values were obtained by subtracting the output power less of C_{SS}=4700pF from that of C_{SS}=10000pF. The result were approximately equal to the loss power of C_{SS}=5300pF.

When the main switching elements are turned off, the charge Q_{SS} of the capacitor C_{SS} in the switched snubber is given by the equation (15), in terms of the drain-source voltage of the main switching elements E_{DS}.

$$Q_{SS} = C_{SS} E_{DS} \qquad \cdots\cdots\cdots(15)$$

The charge Q_{SS} flows through into the forward biased resistance of the drain-substrate PN junction, R_{SS}, and the equivalent resistance of the main switching elements, R_{EQ}. At the time just before the main switching elements turn on, the charge voltage across C_{SS}, which is equal to the voltage across the main switching elements is decreased by the current flowing through the N-channel MOS-FETs. At this time, the on voltage across the drain-source of the main switching elements, $V_{DS}(t)$ is given by the equation (16).

$$V_{DS}(t) = \frac{R_{EQ}}{R_{SS}+R_{EQ}} E_{DS} e^{-\frac{t}{C_{SS}(R_{SS}+R_{EQ})}} \qquad \cdots\cdots\cdots(16)$$

where R_{SS} is the equivalent on resistance of the PN junction between drain and substrate of the N-channel MOS-FET when the PN junction is forward biased. R_{EQ} is the equivalent on resistance of the main switching elements when the gate signal raises as the main switching elements turn on. Therefore, this resistance is normally larger than the equivalent ON-resistance of the main switching elements. Furthermore, the impedance of the load is larger than R_{EQ} plus R_{SS}, and it can be disregarded.

In the voltage waveform across the main switching elements of Figure 5, the voltage across the main switching elements at

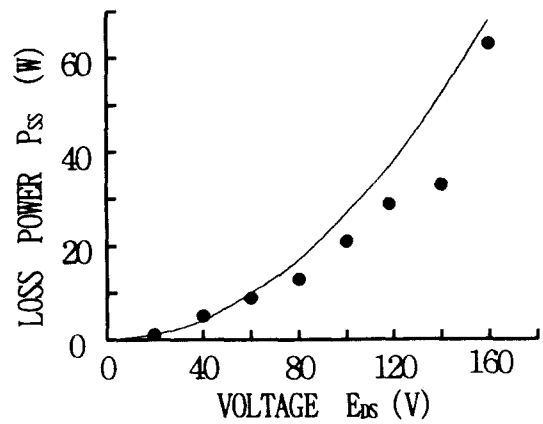


Figure 6. Power loss by the current flowing through the capacitor C_{SS}.

the time just before they turned on, E_{DS}, was 80 V, the voltage across the main switching elements, $V_{DS(0)}$, was 30 V, the time, t_{SS} is 100 ns, and the capacitance, C_{SS}, was 10000 pF. The on voltage across the main switching elements, $V_{DS(t)}$, is given by equations (17) and (18). Where, t_1 and t_2 are the 10 % and 90 % of the time at which the capacitance C_{SS} is fully stored, respectively.

$$V_{DS}(t_1) = 30 \times (1 - 0.1) = 30 \times 0.9$$

$$= \frac{R_{EQ}}{R_{SS} + R_{EQ}} E_{DS} e^{-\frac{t_1}{C_{SS}(R_{SS}+R_{EQ})}}$$

$$= 30 \times e^{-\frac{t_1}{1.0\times10^{-8}\times(R_{SS}+R_{EQ})}} \quad \cdots\cdots\cdots(17)$$

$$V_{DS}(t_2) = 30 \times (1 - 0.9) = 30 \times 0.1$$

$$= \frac{R_{EQ}}{R_{SS} + R_{EQ}} E_{DS} e^{-\frac{t_2}{C_{SS}(R_{SS}+R_{EQ})}}$$

$$= 30 \times e^{-\frac{t_2}{1.0\times10^{-8}\times(R_{SS}+R_{EQ})}} \quad \cdots\cdots\cdots(18)$$

$$t_2 - t_1 = t_{SS} \times 0.8 \quad \cdots\cdots\cdots(19)$$

$$= 100 \times 10^{-9} \times 0.8$$

R_{EQ} is assumed constant. From the equations (17) through (19), R_{SS} and R_{EQ} are given by the equations (20) and (21).

R_{EQ}=1.4 (Ω)

R_{SS}=2.3 (Ω)

Therefore, when the main switching elements turn on, the ON-resistance of the main switching elements, R_{EQ}, is 1.4 Ω, and the ON-resistance of the switched snubber, R_{SS}, is 2.3 Ω when the PN junction of MOS-FET is forward biased.

Figure 7 shows the output power and power conversion efficiency of the inverter showing the effect of the switched snubber on the power losses. In Figure 7, if the capacitance is large, the power conversion efficiency is low. Therefore, a large capacitance value of the switched snubber depresses the surge voltage effectively.

5. Conclusion

The cause of generating the surge voltage across the switching elements was studied. The effect of the switched snubber using an N-channel MOS-FET on depressing the surge voltage appearing across the switching elements was also studied. The calculated and measured surge voltage waveforms were shown to demonstrate the depression of the surge voltage. The current flowing through the switched snubber constructed using an N-channel MOS-FET was calculated,

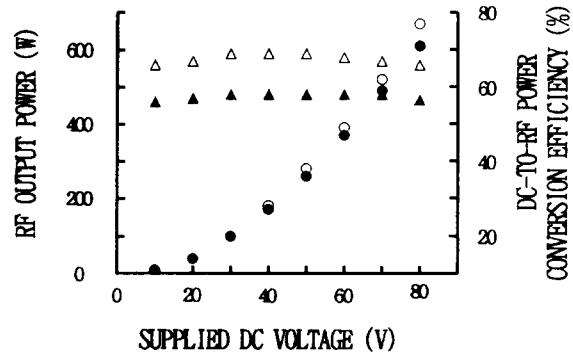


Figure 7. Output power and power conversion efficiency.

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