On-board Computer Design for KITSAT Systems

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SaTReC successfully launched two microsatellites named KITSAT-1 and 2 in 1992 and 1993, respectively and has operated them since then. As multimission experimental satellites, KITSAT-1 and KITSAT-2 have carried various kinds of experimental payloads such as store-and-forward packet communication, earth imaging, and radiation monitoring. These two satellites are controlled by a carefully designed on-board-computer(OBC). As the master mission control computer, OBC manages all the housekeeping works including ground-to-spacecraft communication, attitude control, bus subsystem management, and payload control. In this paper, we discuss in-orbit operation results of KITSAT-1, 2 OBC and describe the design issues on KITSAT-3 OBC. After the successful operations of KITSAT-1 and 2, SaTReC has set up a next stage development plan for a small satellite called KITSAT-3. KITSAT-3 is designed to experiment on several valuable space technologies including 3-axis stabilized attitude control, solar panel deployment, high speed transmitter, and high resolution CCD camera. The KITSAT-3 OBC is different from KITSAT-1, 2 OBCs in several aspects. It should be operated in higher speed to control various attitude sensors and actuators such as star sensor, rate gyroscope, and reaction wheels, in addition to its housekeeping tasks. The CPU speed is determined through its throughput estimation. Even though the single event upset(SEU) analysis from KITSAT-1, 2 OBC memory shows that current error detection and correction(EDAC) scheme could successfully recover almost all the memory upsets induced by space radiation environment, EDAC is modified to detect double errors and implemented on a EPLD device to reduce its space and weight. Dynamic EDAC WASH rate is adopted by software control. The whole software stack is designed for efficient, reliable, portable spacecraft operations. We analyze KITSAT-1, 2 OBC software operation results and finally describe KITSAT-3 OBC software design issues.