Reliability Issue in LOC Packages

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Abstract

Plastic IC encapsulation utilizing lead on chip(LOC) die attach technique allows higher device density per unit package area, and faster current speed and easier leadframe design. Nevertheless, since the top surface of the chip is directly attached to the area of the leadframe with a double-sided adhesive tape in the LOC package, it tends to be easily damaged by the leadframe, leading to limitation in its its utilization. In this work, it is detailed how the damage of the chip surface occurs, and it is influenced and improved by the LOC construct.

Experiment

The reliability test in this work is confined to thermal cycling. Predetermined time required for the qualification of reliability is 1000 cycles for T/C tests. For each set of experiments nominally identical specimens were placed in the thermal cycle chamber, then individuals were functionally tested after predetermined periods (i.e. 150, 300, 600, 1000 cycles). Test specimens underwent thermal displacement-induced fatigue at temperature ranges of from -65°C to 150°C with 30min. time period. Once any functional failure was found, the corresponding specimens were decapped and examined under an optical microscope(OM) and scanning electron microscope(SEM) to identify the failure region. Since the precise site of cracking was hardly detected because the failed specimens mainly contain well-developed cracks, a large number of specimens were required to investigate the crack nucleation site. Two package types assembled in a LOC technique, small outline J-leaded(SOJ) packages and thin small outline packages(TSOP), were tested. These LOC packages are typically combined as epoxy mold compound, 42Ni-Fe alloy lead frame, double-sided adhesive tape and etc.

Results

Experimental works indicate that the functional failure associated with a passivation break took place during thermal cycling(T/C) tests. To give a great insight into the passivation cracking phenomenon, a mechanism related to it was established through stress simulation using the finite element method(FEM) and it was shown that the double -sided adhesive tape used for the attachment of the leadframe to the chip surface plays a significant role in defining degree of the passivation damage. That is, the study of the passivation susceptibility to cracking revealed that the passivation cracking occurence is a strong function of the shear stress induced by thermal displacement mismatch between LOC packaging materials. Experimentally, it is shown that the thermomechanical stability of LOC packages can be considerably enhanced by the reduction of the shear stress induced by the tape, which is investigated as the primary cause of a passivation crack.

Conclusions

Reliability of the high density memory devices assembled in SOJ packages adopting a LOC die attach technique was shown to be significantly improved through the modification of the lead frame design such as the reduction of the tape thickness or tape area.