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Parallel Fuzzy Information Processing System

- KAFA : KAist Fuzzy Accelerator -

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ABSTRACT

During the past decade, several specific hardwares for fast fuzzy inference have been developed. Most of them are dedicated to a specific inference method and thus cannot support other inference methods. In this paper, we present a hardware architecture called KAFA(KAist Fuzzy Accelerator) which provides various fuzzy inference methods and fuzzy set operators. The architecture has SIMD structure, which consists of two parts; system control/interface unit(Main Controller) and arithmetic units(FPEs). Using the parallel processing technology, the KAFA has the high performance for fuzzy information processing. The speed of the KAFA holds promise for the development of the new fuzzy application systems.

1. Introduction

Since Zadeh introduced the fuzzy set theory in 1965, fuzzy logic has attraction in which the processes are too complex to analyze by conventional quantitative techniques and in which the available sources of information are interpreted qualitatively, inexactly or uncertainly[1]. During the past decade, fuzzy theory has been applied to solve real-world problems in such areas as control, operations research, pattern recognition and expert systems [2][3][4]. Fuzzy control especially has been actively applied and gotten the satisfactory results in the industrial fields. In those areas, fuzzy information has been processed by software on the conventional general purpose microprocessors. Though it is very flexible to develop the fuzzy applications with software-based approach, it costs a lot of computation time because fuzzy set operators are not directly supported by general purpose microprocessors and there are a large amount of data in the fuzzy information processing.

In the application areas requiring high speed processing such as real-time control, some special purpose microprocessors and some fast fuzzy inferencing systems have been developed[5][6][7]. However, they are limited in generality, that is, there is no flexibility in inference methods. Moreover it can not be used for other areas of fuzzy information processing, which don't include inference.

In this paper, we describe a hardware architecture called KAFA(KAist Fuzzy Accelerator) for the fuzzy information processing based on fuzzy logic and fuzzy set theory. The architecture has SIMD structure, which consists of two parts; system control/interface unit(Main Controller) and arithmetic units(FPE: Fuzzy Processing Element). It provides various fuzzy set operations as well as various inference functions. The first prototype of KAFA is implemented by using FPGA chips, which contains 128 FPEs.

The next section briefly reviews the fuzzy set operations and the fuzzy inference, and then, section 3 describes the configuration of the KAFA. Section 4 presents the performance evaluation of fuzzy set operations and fuzzy inferences for the prototype of KAFA.

2. Fuzzy Theory

2.1 Fuzzy set operation

Let A be fuzzy set in a universe of discourse U. Fuzzy set A can be represented by a vector of membership values which takes values in the interval [0.1] as follows:

$$A = \sum_{i=0}^{n} \mu_A(u_i) / u_i = (\mu_A(u_1), \mu_A(u_2), \ldots\ldots, \mu_A(u_n))$$

where element u_i is represented by i-th position of U. According to the interpretation of fuzzy set as an extention of the ordinary set, T-norm, T-conorm and negation function as intersection, union and complement of fuzzy sets, respectively. A variety of fuzzy set operators have been proposed by many researchers[8][9].

Table 1. Basic Fuzzy Set Operators

	product(T-norm)	sum(T-conorm)
logical	$a \wedge b = \min(a, b)$	$a \vee b = \min(a, b)$
algebraic	$a \bullet b = ab$	$a + b = a + b - ab$
bounded	$a \otimes b = 0 \vee (a + b - 1)$	$a \oplus b = 1 \wedge (a + b)$
drastic	$a \dot{\wedge} b = a$ if $b = 1$ b if $a = 1$ 0 otherwise	$a \dot{\vee} b = a$ if $b = 0$ b if $a = 0$ 0 otherwise

Table 1 shows the widely accepted basic fuzzy logic operations. Logical operators have been used in most of fuzzy systems because of their computational simplicity. However other type of fuzzy set operators may work better in some situation. It is important to offer the capability of selecting the fuzzy set operator that can be well suited for the given problems.

2.2 Fuzzy inference

Zadeh proposed a computational procedure for fuzzy inference which consists of an implication function and an inference rule called compositional rule of inference. Let us consider the following general form of fuzzy rules of which the antecedent and the consequence contain fuzzy terms:

rule 1 : If x is A_1 and y is B_1, then z is C_1
rule 2 : If x is A_2 and y is B_2, then z is C_2
... ...
rule n : If x is A_n and y is B_n, then z is C_n

where A_i, B_i and C_i are fuzzy terms. The fuzzy rule is transformed into a fuzzy relation R_i and is defined as:

$$\mu_{R_i} = \mu_{(A_i \text{ and } B_i \longrightarrow C_i)}(u, v, w)$$

$$= [\mu_{A_i}(u) \text{ and } \mu_{B_i}(v)] \longrightarrow \mu_{C_i}(w)$$

where → denotes a fuzzy inplication function. There are many ways to define a fuzzy relation according to the type of implication functions[10].

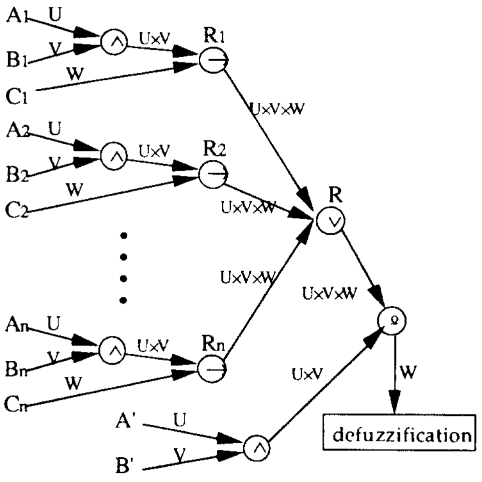

Figure 1. Fuzzy inference

Given a fact A', B' and relation R, then, the result C' is inferenced by the compositional rule of inference, that is

$$C' = (A', B') \text{ o } R$$

where o is a sup-✻ compositional operator. The most frequently used sup-✻ compositional operator is Zadeh's max-min composition. The result C' is defuzzified to a crisp number, which then can be used as the control action. The commonly used strategies are the max criterion, the mean of maximum and the center of area.

3. Configuration of KAFA

The major hardware components in KAFA are shown in figure 2. The Fuzzy Processing Element(FPE) array with 128 FPEs operates on SIMD mode. Each FPE contains a 1024-byte RAM for the storage of knowledge base. Each FPE is a word-slice microprocessor connected to its both side neighbors. The first and the last FPE are connected to Main Controller so that the array topology forms the ring network. The FPE array has the cycle time of 200ns. The control unit(Main Controller) is microprogrammable. It supervises the FPE array processing, controls the interface with the host system and broadcasts data across the FPE array.

The host system is a front-end microcomputer. It downloads data into the FPEs and microprograms into the Main Controller. At present, an IBM PC486 is used as the host system.

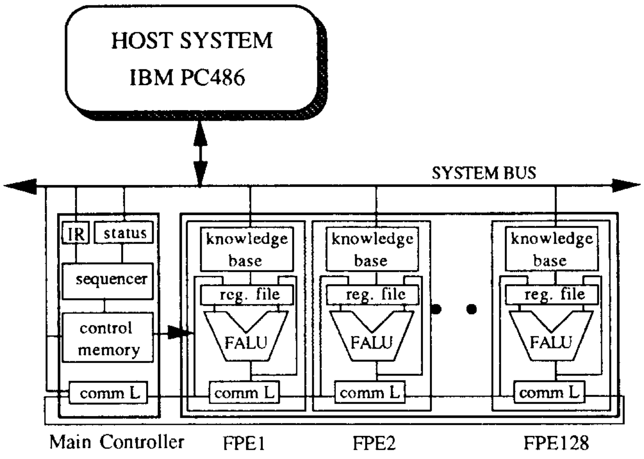

Figure 2. Overall configuration of KAFA

- **Data Format** - The KAFA deals with discrete fuzzy set. As seen in Figure 3, a continuous fuzzy set is sampled at n elements and then fuzzy set is represented by a n-ary vector where each element is a membership value. The value of membership function is represented by 8 bits, so it has the precision of 128 levels. For example, membership value 0 corresponds to Hx00 and 1 to Hx80.

In the KAFA, a fuzzy set is represented by the fixed-point positive value, so 8 bits membership value has the range from 0(Hx00) to 1+127/128(HxFF). Then, during the fuzzy operation, intermediate results may exceed 8 bits capacity and thus overflow occurs. To solve this problem, the sequence of operation is properly rearranged. For example, in the algebraic sum((A+B)-(AB)), the intermediate result A + B may exceed 8 bits, but the rearranged sequence(((1 - B) * A) + B) has no problem.

- **Main Controller** - Main Controller of KAFA plays the role to interface with the host system and to control the operations of the FPEs. Main Controller is a microprogrammable control unit which can flexiblely define the instruction set for fuzzy operations. The microinstructions which are stored in the control memory, are 43 bit-wide and contains the information for the FPE operation, the data communication and the control of the sequences of

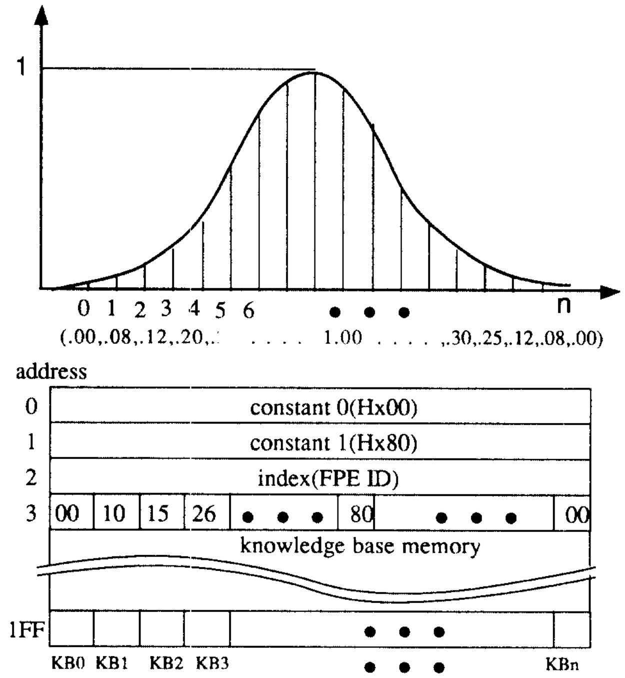

Figure 3. Data structure

the microprogram. All instructions can be read and executed within 200ns.

The control memory contains a number of system routines and user written routines to perform the various fuzzy set operations.

FPE	stat.	com.	KB	BR	NA
(15)	(1)	(3)	(12)	(2)	(10)

The value in ( ) indicates the number of bits

Figure 4. Microinstruction format

- **FPE** - The FPEs are word-slice processors for processing membership values. The clock rate is 10 MHz and 128 FPEs operate in parallel, so KAFA has a very high processing speed. Figure 5 shows a FPE unit which consists of a FALU(Fuzzy ALU), a knowledge base memory, a register file, conditional flags and a communication link. The control signals from the Main Controller are broadcast to all FPEs, and then all FPEs perform a fuzzy set operation synchroneously.

In the internal operation of FPE, it has three sections that can operate in parallel; FALU operation, memory read/write and communication.

The FALU provides the 11 basic instructions. Each instruction is performed at one clock cycle. The fuzzy set operations are microprogrammed using those instructions. Table 2 summarizes the instruction set of FALU.

In the SIMD structure, Main Controller sends the same instruction to all FPEs and each FPE executes the instruction with one element of fuzzy set. However, there are exceptional cases, each FPE can execute differently according to conditional flags. The MOV.flg and TRN.flg instuction can be associated with a previously executed comparision or other logical operation so that only those FPEs satisfying the logical condition are engaged in the operation.

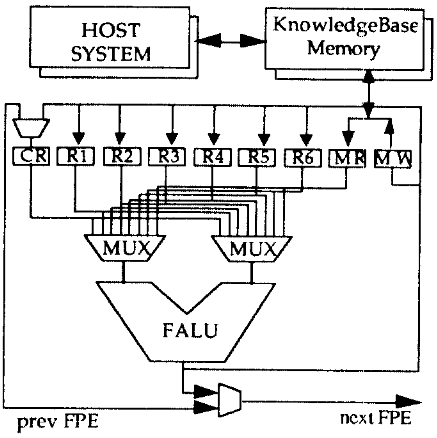

Figure 5. FPE unit

Table 2. FALU instruction set

MNEM.	FUNCTION	CODE				FLAG
NOP	no operation	00XX	XXX	XXX	XXX	- - -
ADD	add	0100	S1	S2	D	C Z O
ADC	add with carry	0101	S1	S2	D	C Z O
SUB	subtraction	0110	S1	S2	D	C Z O
–	–	0111	XXX	XXX	XXX	- - -
MIN	minimum	1000	S1	S2	D	E L G
MAX	maximum	1001	S1	S2	D	E L G
SHL	shift left	1010	S1	S2	D	C Z O
SHR	shift right	1011	S1	S2	D	C Z O
MOV	move	1100	S1	000	D	- Z O
MOV.C	condit. move(carry)	1101	S1	S2	D	- Z O
MOV.Z	condit. move(zero)	1110	S1	S2	D	- Z O
MOV.O	condit. move(one)	1111	S1	S2	D	- Z O
TRN	transfer	1100	S1	100	XXX	- - -
TRN.C	condit. transfer(carry)	1100	S1	101	XXX	- - -
TRN.Z	condit. transfer(zero)	1100	S1	110	XXX	- - -
TRN.O	condit. transfer(one)	1100	S1	111	XXX	- - -

- **Communication** - A unique identification(ID) number is assigned to each of the FPE. The ID number is used for the communication between FPEs. Each FPE checks its own ID number and then determine whether to pass the data from the previous FPE or tranfer its own data.

The Communication link is used for the data broadcasting and the defuzzification. Main Controller broadcasts the input data to all FPEs. The propagation delay needed for the last FPE to receive the input data exceeds one clock cycle. As the transfer instruction is repeatly executed, all FPEs can receive the valid input data.

4. Evaluation of the KAFA

4.1 Fuzzy set operation

Assume that a fuzzy set is represented by 128 elements and each element is repersented by 8 bits and stored the knowledge base memory of each FPE. For the situation, KAFA at 10MHz shows the performance given in Table 3.

The FLOPS is an abbreviation of Fuzzy Logic Operation per Second, i.e. the KAFA can perform 640 million minimum operations per second and 160 million bounded sum operations per second. The algebraic operation is relatively slow because of multiplication. At present, we are trying to improve the speed of multiplication.

Table 3. The performance of fuzzy set operation

	product(T-norm)	sum(T-conorm)
logical	640 MFLOPS	640 MFLOPS
algebraic	20 MFLOPS	19 MFLOPS
bounded	128 MFLOPS	160 MFLOPS
drastic	160 MFLOPS	160 MFLOPS

4.2 Fuzzy inference

Assume that each fuzzy rule is of the form(A_i and $B_i \rightarrow C_i$) and the input values A' and B' are crisp values. As shown in Figure 6, each data path consists of four phases.

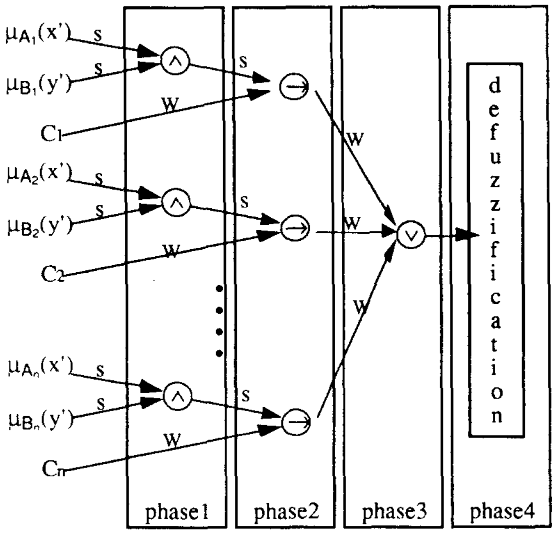

Figure 6. Fuzzy inference

- phase 1 : scalar - to - scalar operation
- phase 2 : scalar - to - vector operation(implication)
- phase 3 : vector - to - vector operation(aggregation)
- phase 4 : vector operation(defuzzification)

The phase 1 is processed in the host computer and the phase 2 and 3 are processed in the FPEs under the control of Main Controller. The processing time of the phase 2 depends on the type of implication functions. The most commonly used implication function, Mamdani's Max-Min method is performed at one clock cycle. The phase 4 is the defuzzification phase.

Table 4. Performance of fuzzy inference(cycle)

Implication function	phase 2	phase 3
mini operation rule	100	100
product operation rule	3300	100
arithmetic rule	300	100
maximum rule	300	100
boolean rule	200	100

defuzzification	phase 4
max criterion	31
mean of maximum	33
center of area	529

(* 1 cycle == 200ns)

When the number of the rules is 100 and all rules contribute to the final conclusion, the performance of several inference methods including defuzzification is shown in Table 4.

5. Conclusion

In the area of applications required high speed processing such as real time control, many hardware implementations have been proposed. To speed up the inference process, most of these proposals transform the basic inference procedure into hardeware devices and/or store partial results for runtime usage to a large amount of memory, i.e. lookup table. So these hardware implementations have restriction on the inference methods and the fuzzy set operations. In the meantime, the different kind of inference methods and/or fuzzy set operations are needed depending on the applications. Thus the existing hardware implementations have difficulty in supporting this kind of flexibility.

In this study, we design and implement a new hardware architecture, which provides various fuzzy inference methods and fuzzy set operations. Parallel processing technology is used for achieving the high speed processing. The speed of the KAFA holds promise for the development of the new fuzzy applications such as real time image processing, fuzzy databases and robotics, etc..

Future research will be directed towards the development of fuzzy applications at new area and the algorithmic improvements which will reduce the runtime of the KAFA.

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