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A VLSI-CMOS PROGRAMMABLE MEMBERSHIP FUNCTION CIRCUIT: THE BASIC BLOCK OF FUZZY PROCESSING

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ABSTRACT

The fuzzifier circuit DPFC_7 is presented. Its features are: programmable membership function, CMOS digital interface, analog and current mode internal processing and integrability without external components. It has been designed to obtain a basic efficient block for fuzzy processing, to be included in a future architecture.

1 INTRODUCTION

The first question to deal when we attempt to process fuzzy information is to represent it. In [Ruiz92] we presented the first ideas about a fuzzy processing approach different than the previous known. The start point is the great quantity of information that one membership function involves. The way to process it efficiently is to codify the trapezoidal functions in 12 bits, called the CMF (codified membership function). But we need a "decoder" to interpret it. In [Ruiz91] a first version of this circuit, the analog PFC_6, was presented. Now we have improved it, obtaining the DPFC_7 (Digital Programmable Fuzzifier Circuit). The design criteria, circuit description, prototype VLSI implementation and test results are presented next.

2 OBJECTIVES

- To dispose a hardware module that implements the processing approach of [Ruiz92], decoding a CMF and processing it by the fuzzify operation (given a fuzzy set and a domain element, to obtain its membership degree).

- This module must be faster than the pure digital approach [Togai87], where the membership function is bit mapped and stored in a RAM.

- The design must be modular and have a good interface in order to be the base of a fuzzy architecture.

3 DESIGN CRITERIA

Analog vs. digital: The internal operations are easily implemented in analog and current mode. However, the external interface is digital to avoid current degradation and to connect with standard CMOS blocks.

Speed vs. precision: In this version the speed is not the main objective, although the delay times are measured. The output precision and definition of sampling range scales are guaranteed first.

4 CIRCUIT INTRODUCTION

The DPFC_7 (fig. 5.1) performs a simple membership operation. In figure 4.1 a trapezoidal

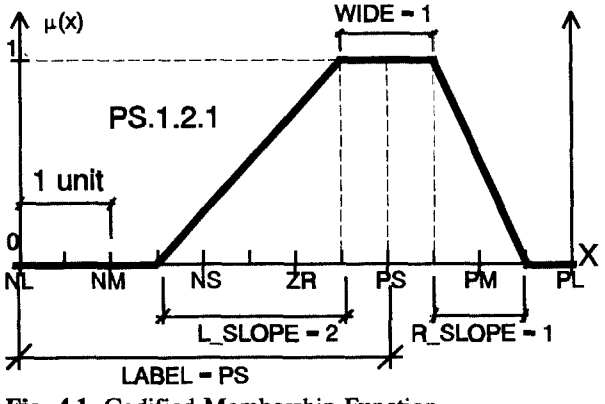


Fig. 4.1. Codified Membership Function.

membership function may be seen. The X axis is the elements domain, represented in current mode as the [0μA, 60μA] interval. The input x is sampled each 2μA, obtaining 31 samples codified in a 5 bit bus (x[0:4]). The fuzzy interval [0,1] in the Y axis (membership degree) is represented in current mode as the [0μA, 49μA] interval (output Io). It is sampled each 7μA, obtaining 8 samples in a multivaluated degree way (bus D[0:6]). The membership function is codified by 4 parameters (B, W, L, and R) whose values are expressed in X units. Each

unit is equal to 10μA or 5 samples. These parameters are codified in 3-bit buses.

5 CIRCUIT DESCRIPTION

The PFC is shown in figure 5.1. The inputs and outputs are digital and CMOS compatible, with the exception of Io (analog in current mode), VGx, VGlabel, and VGd, these three last (analog in voltage mode) being inputs that adjust some gate voltages. The programmable feature is due to the possibility of changing the CMF buses. The internal process is analog (figure 5.2), carried

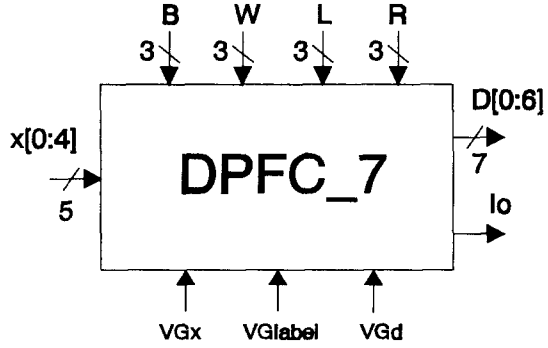


Fig. 5.1. External block of DPFC_7.

in the blocks MLT_D_5. Before and after these blocks there are input (DAC's & ESP_N_CASC) and output blocks (CUANT_7) that perform the analog and digital conversions, in addition to adding or subtracting the corresponding currents. Thereafter, the sampling of both X and Y axes is made by these input and output blocks.

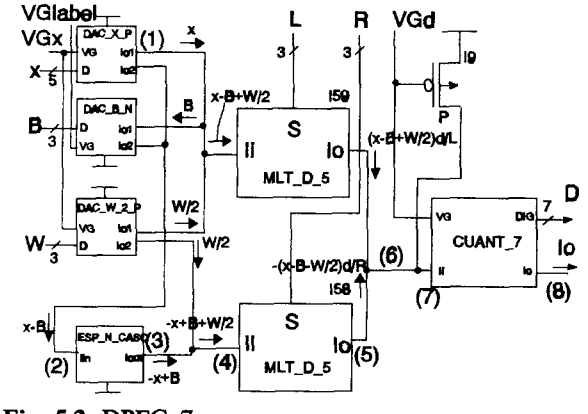


Fig. 5.2. DPFC_7

The steps of processing the right side of the membership function in current mode may be seen in figure 5.3, where there are represented the current through each numbered branch of the figure 5.2 circuit:

STEP (1): A simple y=x function is the output from DAC_X_P to the next node, input of ESP_N_CASC and also output of DAC_B_N.

STEP (2): DAC_B_N subtracts the current value B, resulting in a vertical shift.

STEP (3): The block ESP_N_CASC is a current mirror

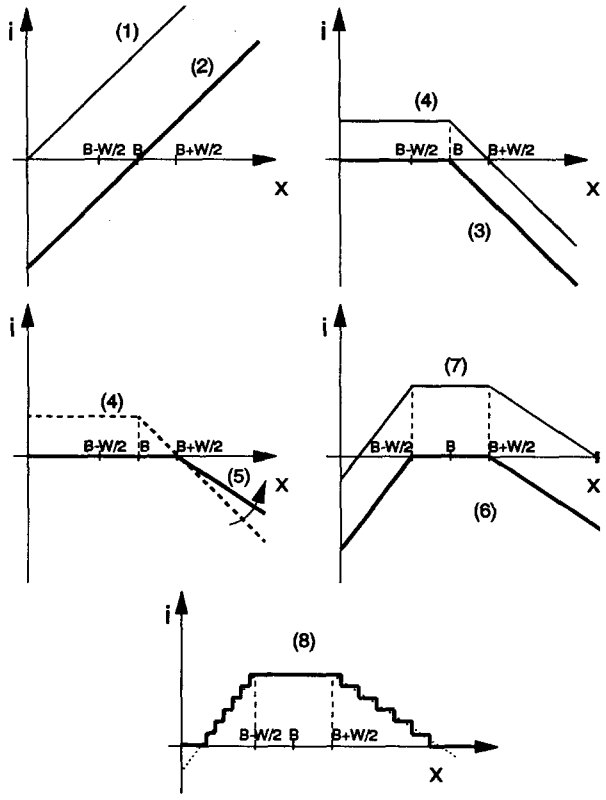


Fig. 5.3. Stages of internal processing of the membership function.

that performs two operations: the "cut" of the negative currents and the change of the current direction. The resulting negative segment has slope -1.

STEP (4): The module DAC_W_2_P adds the parameter W/2.

STEP (5): (module MLT_D_5) First the cut of positive currents, and second, amplification and change of the slope, depending on the parameter R.

STEP (6): The both branches (L and R) of the function are added. The zero segment of one branch has no effect on the other.

STEP (7): The PMOS I9, behaving as current source, adds the parameter d, value of degree "1".

STEP (8): The negative currents are cut (CUANT_7) and the current is made discrete, passing to a multiple-valued domain (8-valued). This is the current going out from Io. In addition, an analog to digital conversion is made, obtaining the decodified digital bus D.

Let us stress that the real current flowing through the different branches is slightly different than the ones in fig 5.3 because the cut effects are produced at the input of the blocks, and so affecting the previous step. The three input converters (DACs) are composed by weighted current sources, each of them controlled with a

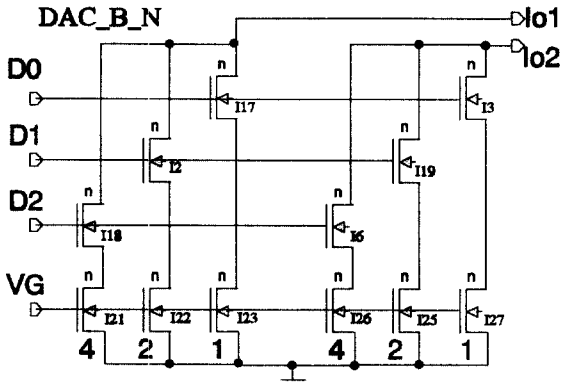


Fig. 5.4. DAC_B_N.

pass transistor. DAC_B_N and DAC_W_2_P may be seen in figures 5.4 and 5.5. ESP_N_CASC is a n-type

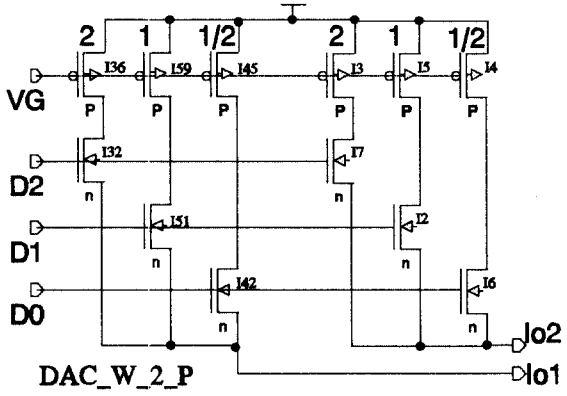


Fig. 5.5. DAC_W_2_P.

current mirror designed with 4 nmos, connected in two levels of cascade. This connection reduces the output current error.

The core of the DPFC_7 are the multipliers

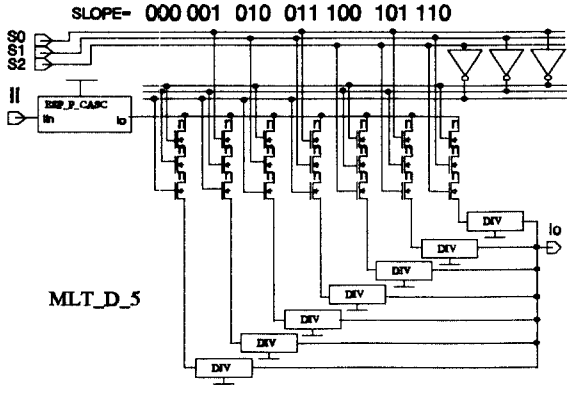


Fig. 5.6. MLT_D_5.

MLT_D_5 (fig. 5.6). Their function is to change the slopes of the membership function to the value according with the parameters L and R. This is made via the amplification of the current in the DIV modules. These are current mirrors with a certain gain, made by the ratio between the input and output channel widths. Each DIV represents a different amplification, and consequently we have a discrete multiplication. There are 7 DIV modules, related to the 7 possible values of the L (R) parameter. The correct DIV module is selected with a multiplexer made with an array of pass transistors, externally connected to the slope parameter L or R. Both multipliers are identical, simplifying the design of the layout cell. The p-type current mirror ESP_P_CASC at the input is necessary for the current cut effect of the step (5) of the figure 5.3.

The last stage is CUANT_7 (fig. 5.7), quantifier and AD converter. The quantization is achieved by making 7 copies of the input current, whose aspect is that of step (7) in figure 5.3. This is made by MespN7casc, a 7-output n-type cascade current mirror, that also cuts the negative input currents, obtaining in this way the lateral segments of membership degree 0. Each one of this 7 copies is "compared" with a threshold current between two adjacent reference current levels of the 7-valued code. If the reference values are Iu, 2Iu, 3Iu,.., 7Iu the threshold currents are 0.5Iu, 1.5Iu,.., 6.5Iu, Iu being equal to 7μA. This comparation is achieved by connecting each output of the mirror to a current source (pmos) that supplies the corresponding threshold value.

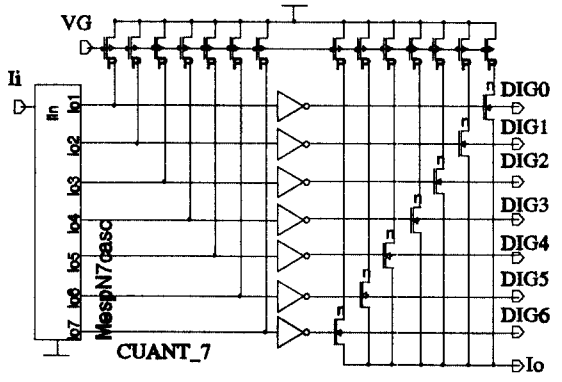


Fig. 5.7. CUANT_7.

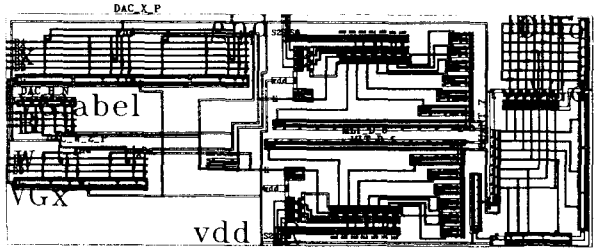
The node is also connected to the input of a logic inverter. Let us see the behaviour of one of these nodes. The working point is determined by the lowest current of both the input and the threshold current, cause their are supplied by MOS current sources. If the input current is lower than the threshold current, the output nmos of MespN7casc makes the pmos source to stay at resistive region, the only point where the pmos characteristic curve can supply the same current (the inverter input current is negligible). This makes the voltage of the node to be high, near vdd, where the resistive region of the pmos takes place. The high value of the voltage feeds the

inverter, obtaining a logic "0" at its output. A similar process occurs when the input current is higher than the threshold one. The inverters outputs are the output bus DIG[6:0]. So this is a decodified digital bus, with 8 levels of membership degree. For example, the degree 4 of membership is represented by the values DIG[6:0]=0011111. The final stage of CUANT_7 is the conversion to current mode. This is made by the addition of 7 identical reference currents (Iu=7μA), each one activated with a pass transistor controlled by the corresponding bus bit. A full membership degree is represented by a 49μA current.

6 VLSI IMPLEMENTATION RESULTS

The DPFC_7 has been designed at layout level (fig 6.1) and integrated via EUROCHIP. Fortunately, in this first prototype there was not any design nor integration errors and the chip has been successfully tested. As the output of DPFC_7 is a digital bus, the precision results are measured as the percentage of correct output degrees related to the theoretical values.

22 different CMFs have been measured, each one containing 31 samples in the X axis. The average



DPFC_7

Fig 6.1. DPFC_7 layout.

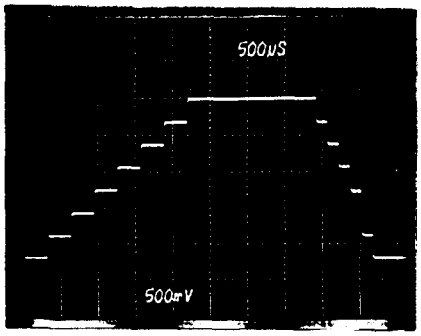


Fig. 6.2. Output of DPFC_7 test.

incorrect levels per CMF is 4.5 (14.4%), almost (99%) the whole of them being ±1 level errors. This means that the output precision is ±1 level. The figure 6.2 shows the output Io through a complete sweep of the X axis at 60kHz of sampling frequency. The programmed CMF is B.W.L.R = 4.2.3.1. The figure 6.3 shows a membership

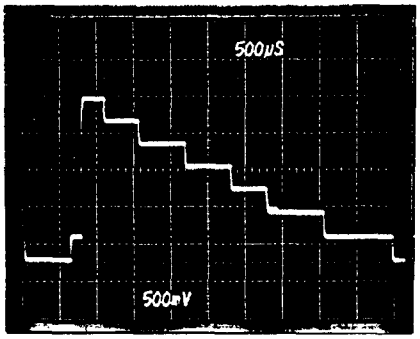


Fig. 6.3. CMF with crisp left slope.

function (1.0.0.5) with the left slope equal to 0 (a crisp slope). This is an example of the chip programmability, that can represent up to 1,010 different CMFs.

The maximum propagation delay (from change in X, B, W, L or R to output) is 10μs. The minimum one is 100ns and the average is 947ns (over 224 measured samples). The operation frequency is consequently 100kHz. The supply margin is from 4.5V to 5.5V and the power consumption is 50mW. The technological process is a 1.5μm Dual Metal CMOS. The area is 6mm^2 including pads and 1.1mm^2 without them. This last can be reduced in approximately 50% area. There are 218 mosfets in the design and the pads ring is composed by both analog and digital pads, with independent supply and ground lines.

7 CONCLUSION

A membership function circuit has been designed, integrated and successfully tested. The key feature is its programmability. The following steps are: to test it in a real system and to redesign it to improve its performance. Now we can use it as a basic design block for making systems that process fuzzy information efficiently.

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