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A HIGH-SPEED FUZZY PROCESSOR USING BIPOLAR TECHNOLOGY

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Abstract: A high speed fuzzy processor using bipolar technology is proposed in this paper. The hardware system uses a high-speed current-mode membership function circuit and normalization technique. The new membership function circuit generates an ideal membership function of the fuzzy set and its circuit is also simple and available for VLSI implementation. Several techniques have been implemented to speed up response of the processor.

The fuzzy processor has been designed and implemented in bipolar circuit technology. The experiments and simulations show that the response speed is below 100ns. It can also be expected that the fuzzy processor can be integrated on one chip and its response time is only about the order of nanoseconds.

I. INTRODUCTION

Since Zadeh proposed the fuzzy set theory and fuzzy logic, many researches on the application of the fuzzy set and fuzzy logic have been done. Especially, fuzzy control systems have recently found various applications. For example, in city subway system, in nuclear reactor control and in automobile transmission control [1]-[3]. These control processors are usually very rapid, proceed without a mathematic model, and are based on an approximate representation of the control surface and its behavior as the system is fed various input values. However, practical control problems require a higher control speed and a smaller controller system. There have been several fuzzy processing system reported [4]-[6].

In this paper, we describe a high speed and high density fuzzy control processor using bipolar technology. The hardware system uses a height-method defuzzification technique, a high speed current-mode membership function circuit and a current-mode normalization circuit combining the MIN circuit. These lead to a high-speed and high-density fuzzy processor.

Instead of using current mirror, we use current-mode wired-sum and wired-subtraction technique in the design of the processor because we found in our simulations that current mirrors tend to be slowest part in the processor. In order to improve input range, and dynamic range, we use base-common technique which inserts base-common transistors between differential pairs and MIN circuits so that the input ranges are increased to ± 5V even higher if needed. The defuzzifier circuit using current mode normalization technique offers a new parallel defuzzy method with high precision and high speed.

The total delay time below 100ns is simulated and measured. It can also be expected to reach a response within the order of nano seconds

II. ARCHITECTURE

we consider a fuzzy controller system that has two inputs x and y, one output z, and n if-then rules. The defuzzification is assumed to be the height-method. The corresponding fuzzy processing architecture is shown in Fig.1.

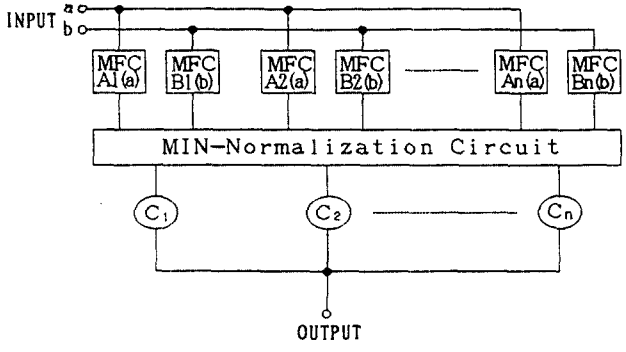


Fig. 1. A fuzzy processing system with height method defuzzification.

Functions in the blocks in Fig.1 are described as following:

A block of the first layer corresponds to one possible of value of one of the linguistic variables in *a* and *b*. For example, if large is one of the value that *a* can take, a block belonging to the first layer computes $\mu_{large}(a)$. An input feeds to all the rules using the clause "*if a is large*" in the *if* part. This function is usually known as the membership function and it specifies the degree to which the given *a* satisfies the quantifier, e.g. *large*.

The second layer is referred to as consequent. It calculates the ratio of the i rule's firing strength to the sum of all rule's firing strength. In other words, it computes the normalized first strength of each rule.

The third layer computes a weight-sum of the second layer. Thus we have constructed a fuzzy processing network which is functionally equivalent to a fuzzy system based on defuzzification of the height method. In our design, the defuzzification of the height method is to be preferred because it is very simple and proved to give the best control [7]. Compared to traditional fuzzy processing system, it allows the minimum number of signal passing stages [6].

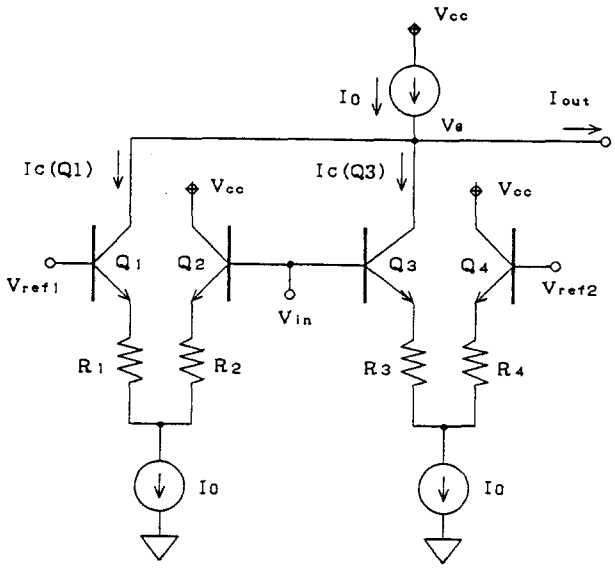


Fig. 2. A membership function circuit without current mirrors.

III. HARDWARE DESIGN

As mentioned above, a fuzzy processing system based on the height method defuzzification consists mainly of membership functions, a normalization function and weight-sum operations. In our previous works, we proposed a fast normalization circuit using parallel MIN circuit technique. It was only 25% of delay time of a membership function circuit. Furthermore, the delay time of the weighted-sum circuits may usually be neglected.

Although several membership function circuits have been reported, they tend to be the slowest part in the whole system. They were usually realized with the combination of differential amplifiers and pnp current mirrors. According to our simulations, the low response speed of the pnp current mirror is due to the source of low speed. In this paper, we describe a new membership function circuit and several techniques are used to improve speed and precision of the membership function.

First, instead of using current mirrors, we use current-mode wired-sum and wired-subtraction in the design of the membership function. Fig.2 shows the membership function circuit proposed here. It consists of two differential pairs biased in V_{ref1} and V_{ref2} ($V_{ref1} < V_{ref2}$), and collectors of Q_1 and Q_3 wired. the output current I_{out} becomes:

$$I_{out} = I_O - I_c(Q_1) - I_c(Q_3). \qquad (1)$$

The input voltage V_{in} is applied to the bases of Q_2 and Q_3. If V_{in} is smaller than V_{ref1}, or larger than V_{ref2}, I_O flows almost entirely through Q_1 or Q_3 and the output current I_{out} is 0.

Otherwise, output gives an ideal membership function of fuzzy set. The width, the height and the type of a membership function can be changed with the biasing current (I_O), the emitter resistors (R_1-R_4) and the reference voltages (V_{ref1} and V_{ref2}) easily.

Furthermore, the quiescent collector voltage, V_{c1} of MIN-Normalization circuit should be:

$$V_{c1} \leqq 2V_{be} \simeq 1.4\,(v) \qquad (2)$$

In order to maintain quiescence of the input pairs for the 5-volt change in the input level, the output voltage, Vout of the membership function circuit should be:

$$Vout \geqq 5(v) \qquad (3)$$

Since the output voltage of the membership function circuit is higher than the quiescent voltage of MIN-Normalization circuit, it is necessary to increase the voltage level between the membership function circuit and the MIN-Normalization circuit, but without changing current level. The low impedance and high speed base-common transistor gives near unit current gain and collector an inherent voltage drop (V_F = 0.7v) below the base voltage V_{BIAS}, as shown in Fig.3. Thus, we have:

$$V_{out} \simeq V_{BIAS} + V_F \qquad (4)$$

By choosing V_{BIAS} larger than 4.3v, the membership function circuit performs properly while the input voltages vary to 5v.

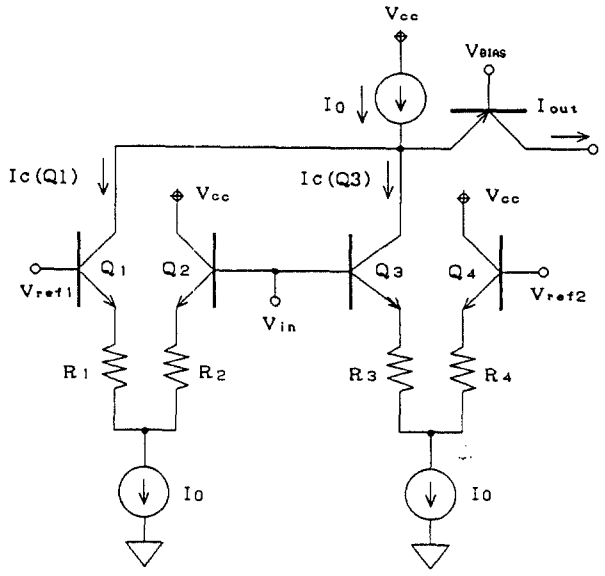


Fig. 3. A high input range membership function circuit with a base-common level shifter.

IV. EXPERIMENTAL RESULTS

Fig.4 shows PSPICE simulation results of the propose membership function circuit. From the simulation results, we can see an ideal membership function is obtained and the circuit performs satisfactory.

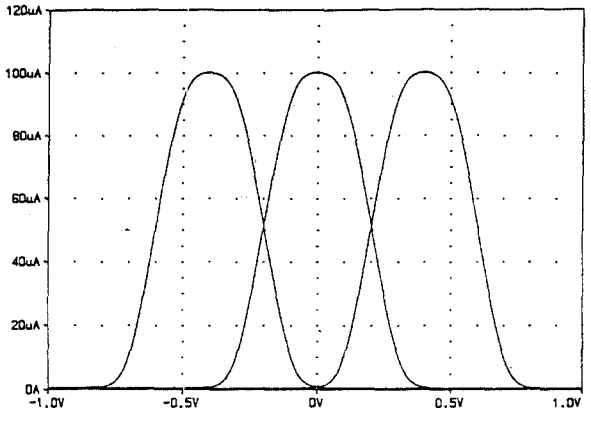
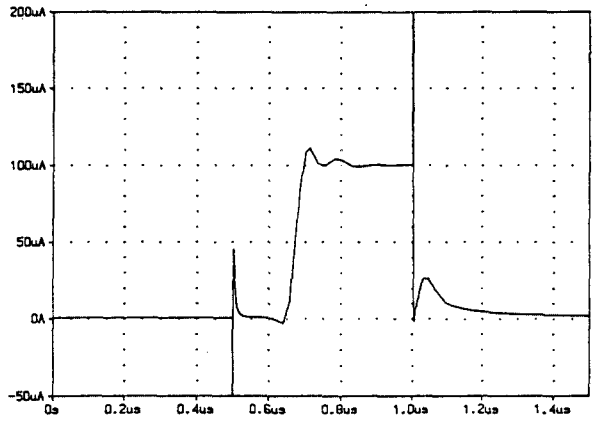
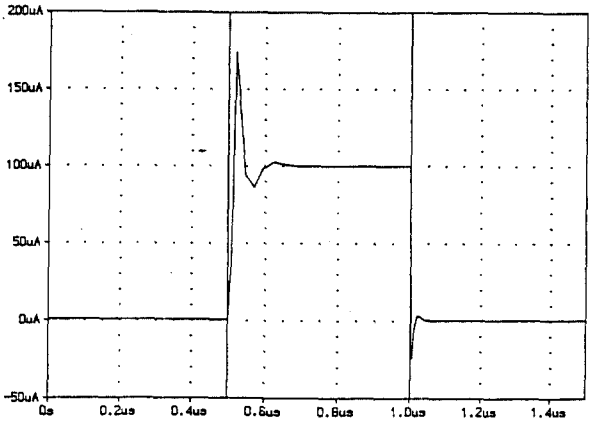


Fig. 4. Simulation results of the proposed membership function circuit.

PSPICE simulations on pulse response were also carried out to both the traditional and proposed membership function circuits. Fig. 5 shows pulse response of the conventional and the proposed membership function circuits. The delay time of the conventional and the proposed circuits are typically about 0.3μs and 0.1μs for rise time, 0.4μs and 0.05μs for fall time respectively.



(a) conventional circuit



(b) Proposed circuit

Fig. 5. Comparison of the pulse response of the membership function circuits while being bias of 100 μ A.

Furthermore, the response speed was improved to about 20ns for rise time and 10ns for fall time, if the bias current is increased from 100μA to 1mA, as shown in Fig. 6.

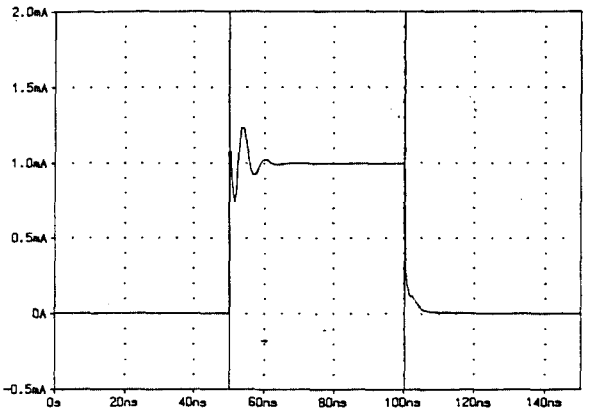


Fig. 6. Pulse response of the proposed membership function circuit while being bias of 1mA.

A 4-input 20 rule based fuzzy processing system using the proposed high-speed membership function circuits and MIN-Normalization circuits was designed and simulated. Simulation results show that the inference time of the fuzzy controller hardware system is within 150ns.

V. CONCLUSIONS

In this paper, we have described a bipolar hardware system for fuzzy processor. A high speed and high density membership function was proposed. Unlike conventional membership function, our membership function circuit involves no current mirror. This makes our membership function circuit simple and what is more important, fast. A delay time of 20ns was measured for the membership function circuits. The speed of the whole system is also improved greatly because the speed of the whole system is largely determined by the speed of the membership function circuit.

The delay time of the whole system was also simulated to be within 150ns. It can also be expected that the bipolar fuzzy processing system can be integrated on a chip and its response time is only in the order of nano seconds.

REFERENCE

[1] Yasunobu, S. and Miyamoto,S., "Automatic trainoperation by predictive fuzzy control," in Industrial Applications of Fuzzy Control, Sugeno, M., Ed. Amsterdam: North-Holland, 1985, pp.1-18.

[2] Bernard, J. A., "Use of rule-base system for process control," IEEE Control Systems Magazine, vol.8, No.5, pp.3-13, 1988.

[3] Kasai, Y. and Morimoto, Y., "Electronically controlled continuously variable transmission," in Proc. Int. Congress Transportation Electronics, (Dearborn, ml), 1988.

[4] T. Yamakawa, "High-speed fuzzy controller hardware system, the Mega-FIPS Machine", Information, Vol.45, pp.113-128, 1988.

[5] F.Ueno, T. Inoue and M. Sakai, "Current-mode analog fuzzy hardware with voltage input interface and normalization locked loop", in Proc. of JTC-CSCC'91, pp.165-170, 1991.

[6] O.Ishizuka, K. Tanno, Z. Tang and H. Matsumoto, "Design of a fuzzy controller with normalization circuits", in IEEE International Conference on Fuzzy systems, pp.1303-1308, 1992.

[7] Mizumoto, M., "Improvement of fuzzy controls (II)," in Proc. of 4th Fuzzy system Symposium, 1988, pp.91-96.