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A Simple Random Signal Generator Employing Current Mode Switched Capacitor Circuit

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Abstract

This paper describes a simple random signal generator employing by CMOS analog technology in current mode. The system is a nonlinear dynamical system described by a difference equation, such as $x(t+1) = f(x(t))$, $t = 0,1,2, \cdots$,where $f(\cdot)$ is a nonlinear function of x(t). The tent map is used as a nonlinear function to produce the random signals with the uniform distribution. The prototype is implemented by using transistor array devices fabricated in a mass product line. It can be easily realized on a chip. Uniform randomness of the signal is examined by the serial correlation test and the χ^2 test.

Key Word: *random signal, CMOS, analog, current mode circuits, chaos, tent map, nonlinear function, time series, uniformly random numbers.*

1. INTRODUCTION

In resent years, as the system becomes more intelligent, analog signal processing, such as neural networks, fuzzy logic systems and chaotic systems, become staged. In these systems, a random signal can be used as a free initial value and a test vector of system tests, etc [1]. In order to built them in the analog system, the random generator constructed with analog circuits is needed.

Several studies that complex time signal sequences can be produced by a simple system employing the deterministic chaos are reported [2],[3]. These systems, however, are constructed with several op-amps and other components, so that these occupies a large area on the chip. By using current mode analog circuit technology, the authors present the new circuit which is as simple as one op-amp circuit and exhibits the same performance to [2],[3].

2. NONLINEAR DYNAMICAL SYSTEM

The system is a one-dimensional dynamical system described by the following difference equation.

$$x(t) = f(x(t)), \quad t = 0,1,2, \cdots \qquad (1)$$

where t is a discrete time, $f(\cdot)$ is a nonlinear function. In this paper, the tent map $T(\cdot)$ (triangular map [4]) described by the following equation is used as a nonlinear function.

$$x(t+1) = T(x(t)) = \begin{cases} 2\,x(t) & (0 \le x(t) \le 0.5) \\ 2 - 2\,x(t) & (0.5 < x(t) \le 1) \end{cases} \qquad (2)$$

where x(t) is defined as [0,1].

This system consists of a nonlinear function unit and a delay unit, as shown in Fig.1. To realize the system in electronic circuits, a nonlinear function circuit implementing the tent map and a delay circuit are needed.

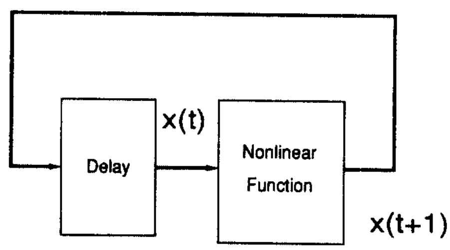

Fig.1 Block diagram of the system.

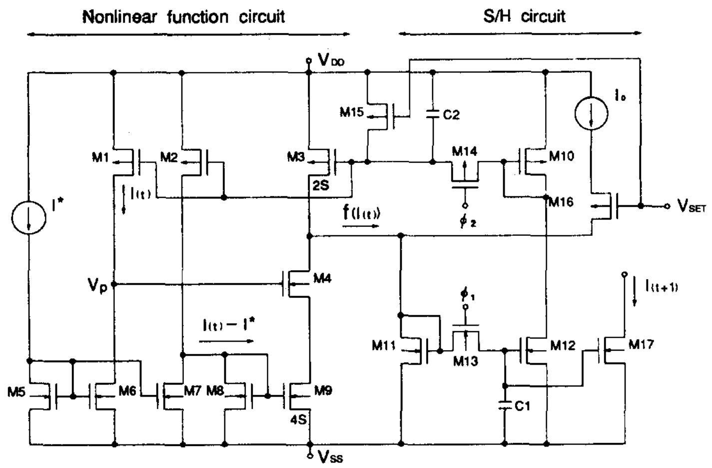

Fig.2 Random signal generator is implemented with current mode MOS analog technology.

3. RANDOM SIGNAL GENERATOR EMPLOYING CURRENT MODE CIRCUIT

A random signal generator is realized by analog MOS circuit in current mode, as shown in Fig.2. Signals are represented by DC currents. The system consists of a nonlinear function circuit, the input-output characteristics of which is described by a triangular function (tent map) and a sample-and-hold(S/H) circuit as a delay element. The S/H circuit can be realized on a simple circuit by using the switched current technique [5],[6].

Nonlinear Function Circuit

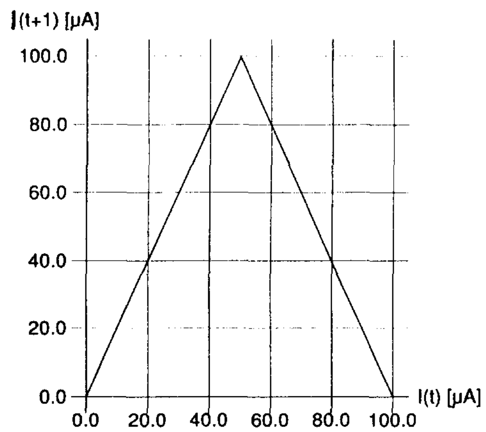

Fig.3 Input-output characteristics of a nonlinear function circuit.

The input-output characteristics of the nonlinear function circuit is shown in Fig.3. The mapping range [0,1] corresponds to the current range [0μA,100μA] . For the current I, equation (2) can be rewritten as

$$
\begin{aligned}
I(t+1) &= 2\,I(t) \qquad (0\ \mu A \le I(t) \le 50\mu A) \\
&= 2(\,2I^*\,) - 2\,I(t) \qquad (50\mu A < I(t) \le 100\mu A)
\end{aligned} \tag{3}
$$

where I^* is a reference bias current that defines a center of the input range, $I^* = 50\ \mu A$ in this circuit .

The left part of Fig.2 shows the nonlinear circuit that consists of nine MOS transistors and one current source.

If I(t) is smaller than the reference current I^* , M6 becomes saturation and V_p becomes closed to $V_{SS}(=0v)$ and M4 becomes off. f(I(t)) equals to the drain current I_{D3} of M3. I_{D3} is twice of the drain current $I_{D1}(=I(t))$ of M1 since the W/L ratio of M3 is twice of M1 [7]. As a result, f(I(t)) = 2 I(t).

If I(t) is larger than the reference current I^* , M1 becomes saturation and V_p becomes closed to $V_{DD}(=5v)$ and M4 becomes on. In this case, f(I(t)) equals to the difference between the drain current I_{D3} and I_{D9}. As the W/L ratio of M9 is four times of M8, I_{D9} is 4 I(t). As a result, $f(I(t)) = 2\,I(t) - 4(I(t) - I^*) = 4\,I^* - 2\,I(t)$.

S/H circuit

S/H circuit consists of five MOS transistors and two capacitors, which employs switched current technique. Capacitors C1 and C2 keep the voltage V_{GS} of M12(M17) and M1(M2,M3), respectively. When the whole circuits are implemented in the monolithic form, these capacitors can be built in as gate capacitors. MOS switches M13, M14 for the sample-and-hold circuit are controlled by two clocks with non-overlapping phases ϕ_1, ϕ_2, respectively.

When M13 is on and M14 is off, M11 and M12 work as a current mirror and C1 is charged up to the V_{GS} that enables M12 to produce a drain current f(I(t)). After M13 becomes off, M12 can continue to produce the current f(I(t)) because C1 holds the voltage. At next step M13 becomes off and M14 becomes on, M10 and M1 work as a current mirror then I(t') = f(I(t)) and C1 is charged up to the V_{SG} that enables M1 to produce a drain current I(t'). In this way, sample-and-hold repeats synchronized to control clocks ϕ_1, ϕ_2.

4. EXPERIMENTAL RESULTS

The simple random signal generator is constructed by the MOS transistor array fabricated in mass production process. As the MOS transistor array exhibits a large leak current, two external 1000pF capacitors are used as hold capacitors C1 and C2.

Fig.4 shows the random signal sequences produced by the system, where the system clock is 1KHz.

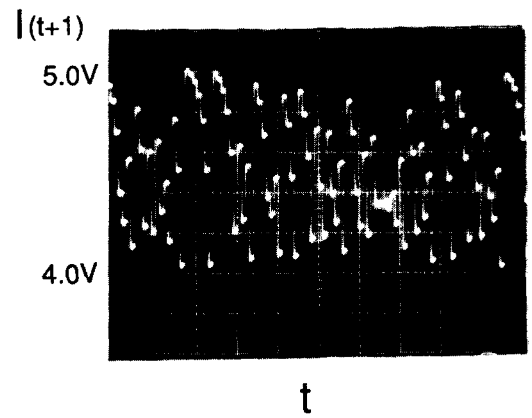

Fig.4 Random signal sequences produced by the simple random signal generator.
(H: 10 msec/div., V: 0.2 V/div.)

To illustrate the performance of the system, these signal sequences are tested by means of the serial correlation test and the χ^2 test [8],[9]. Fig.5 shows a histogram of these signal sequences.

Serial correlation test

On a testing of the serial correlation, the critical region for 5% level of significance is

$$(-\infty, -1.96)\ ,\ (1.96, \infty)\ .$$

Fig.6 shows a result of the serial correlation test. It can be seen from Fig.6 that the signal generated from the system exhibits no correlation with 5% level of significance.

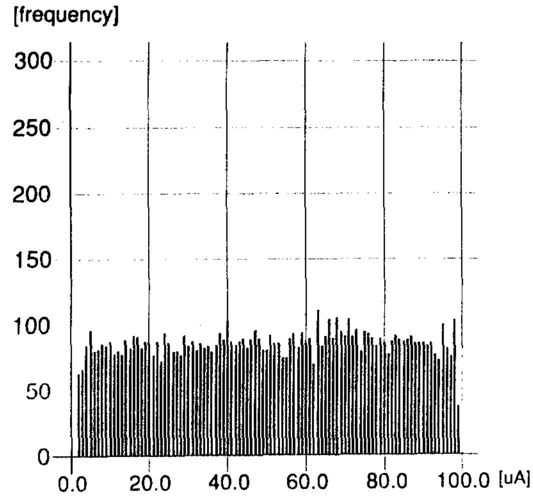

Fig.5 Histogram of the time signal sequences produced by the system

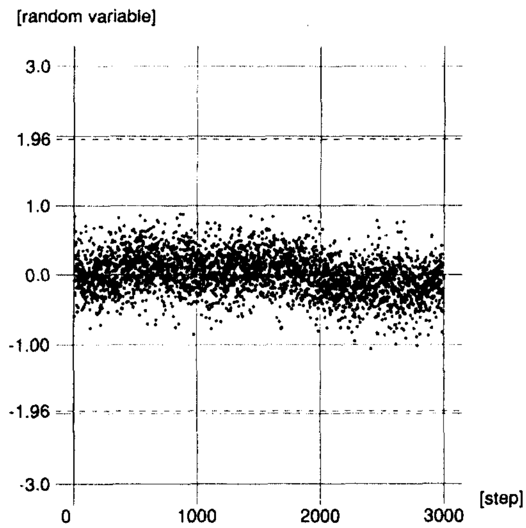

Fig.6 Serial correlation.
(at the level of significance 5%)

χ^2 test

χ^2 test is applied to the signal generated from the system, where the degrees freedom is 30 and the level of significance is 5%. $\chi^2_{30}(0.05)= 42.6$ is calculated from χ^2 distribution.

$\chi^2 = 28.2$ is experimentaly obtained from the signal. As $\chi^2 = 28.2 < \chi^2_{30}(0.05) = 42.6$, the signal produced from the system is uniform at the level of significance 5%.

5. CONCLUSION

A simple random signal generator is implemented with current mode MOS analog technology. The system is represented with a one-dimensional dynamical system using the tent map. The prototype can be constructed with seventeen MOS transistors, two current sources and two capacitors (these can be eliminated in a monolithic chip). The signal produced by this system exhibits uniform randomness.

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