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A Fuzzy Processor Consisting of Memory and Controlling LSI

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ABSTRACT

We have proposed a fuzzy model for behavior of vehicles in the road traffic simulation system with microscopic model for analyzing traffic jam in the broad areas[1],[2]. It can exactly simulate each vehicle's behavior[3]. We propose a new hardware processor to simulate fuzzy decision-making mechanism for its model. This paper describes the functions, performance and structure of the hardware processor.

1. INTRODUCTION

We insist a necessity of macroscopic model for the behavior of vehicles to analyze a road traffic jam. And we point out that it is impossible to simulate exactly the behavior of each vehicle on road traffic jam by statistical and stochastic methods. If simulating the movements of vehicles by a vehicle model with driver's decision-making mechanism, it will be able to analyze more exactly mechanism of road traffic jam[1].

Accordingly, we propose FMV(Fuzzy Model for behavior of Vehicle) and carry out several simulations by the FMV[3]. In these simulations, it turn out that it is impossible to simulate practically the FMVs with several rules at interval-scanning time 0.1 second in a personal computer equipped 5 MIPS degrees.

In practical use, it is necessary to built more accurately a model for the behavior of vehicles by incorporating such many input information in our FMV as distance between leading and following vehicle, vehicle's speed and etc. On the other hand, it is estimated to need a super computer or a connection machine to simulate over 100 FMVs. In fact, it is much load and may be impractical for the kinds of field works where need to analyze the situations of road traffic jam by using these machines.

Almost all the problems to process the much load of fuzzy inference mechanism are generally solved by using a hardware system as a substitute of the accelerator of the conventional computer. We can assure and conclude that it is costly and effectively profitable to develop the most suitably designed hardware processor in particular use which processes the fuzzy inference mechanism.

We propose a new hardware processor to simulate fuzzy decision-making mechanism of FMV. Three essential proposals for developing its processor are proposed in this paper. We construct a LSI which processes the fuzzy decision-making mechanism. The LSI and high-speed memories help to simulate up to 512 FMVs with 128 logics for each FMV, and these are processed within 0.1 second.

The circuits are connected to a conventional micro-processor(68000 family) and controlled by it. These are integrated as a processor to simulate the FMV. A system of routing switch for data transmission and these processors connected in parallel can be able to support strongly road traffic simulation with over 512 FMVs.

2. FUZZY INFERENCE UNIT(FIU)BETWEEN TWO INPUT TERMS

Fuzzy inferences may oblige to obtain the non-fuzzy values by the means of calculating the values of each membership function from non-fuzzy analog data given to inference unit and computing the degree of compatibility for each prepared rule. A FMV requires many fuzzy inferences. If carrying out a series of operations which concern with fuzzy inferences at every scanning time, its execution time is too much to carry out a simulation of practical use.

The first bold proposal is to unfuzzify the results of the inference by carrying out fuzzy inferences substituted calculation of two terms' inferences for ones of the FMV's inferences as shown Fig.1.This means to construct FMV with multistage binomial fuzzy logic in order to transact various restricted road conditions at driving. When we compare with the result of more than three trems' inference and one of only two terms, it can not be proved that two results are constantly equal, for example, as the same as binary logic. Actually, as over 10 input data are necessary for FMV, it is impossible to rule out all the processes such as an additional standard extension of the binary logic, and also almost all the cross terms are nonsense.

So, it is obliged to adopt the cascade logics. In this case, if choosing an intermediate output of two terms' inference as a result with physical meanings, we can substitute two terms' inference for one step of fuzzy inference with multi terms inputted.

On the other hand, an another idea may be not being non-fuzzy, but being cascade connection. But, it is not able to adopt its idea in order to increase the input and output signal of each fuzzy inference, and also be difficult to construct its circuit.

Generally, the two terms' fuzzy inference can be able to give as a function with two variables, if we calculate previously all the values of the non-fuzzy analog output according to two input non-fuzzy ones and keep them. The second proposal is shown in Fig.2. In this case, non-fuzzy analog values in FMV can be represented by at most 8 bits memories. Consequently, all the combinations of two variables are possible to be kept in 16 bits.

In other words, we can substitute a table of 64 K bytes for a fuzzy inference unit (FIU) with two terms' fuzzy inference. As capacity of existing memory IC is larger than this, FMV which needs tens of FIUs is enough to construct by using several Mega-bytes memories. Moreover, in addition to fuzzy inference, FIU is able to carry out some computation concerning to functions with two variables, algebraic operation, decision whether a number is large or small and etc. So, FIU can be able to carry out all the computations, for example, accelerative calculation of vehicles, which are needed in the simulation of FMV by means of table look up. Time to compute them is remarkably faster than one of usual program in software.

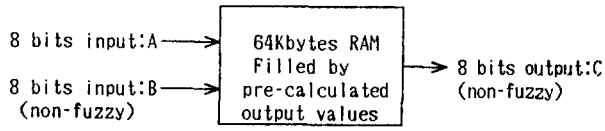

Fig. 2 FIU realized by RAM & controlling LSI

3. METHODS OF CASCADE CONNECTION OF FIU

One FIU can be made of 64 K bytes memories. If we will connect strictly FIUs as looks like a cascade, we must wire 64 K bytes memories unit which is arranged in physical space on hardware. This is not flexible for its connection, and also wiring work is almost impossible to do. So, preparing a configuration table for cascade logic on another memory, referring this, and moving the data from FMV to FIU, we are able to construct virtual cascade logic. This is the 3rd bold proposal in this paper.

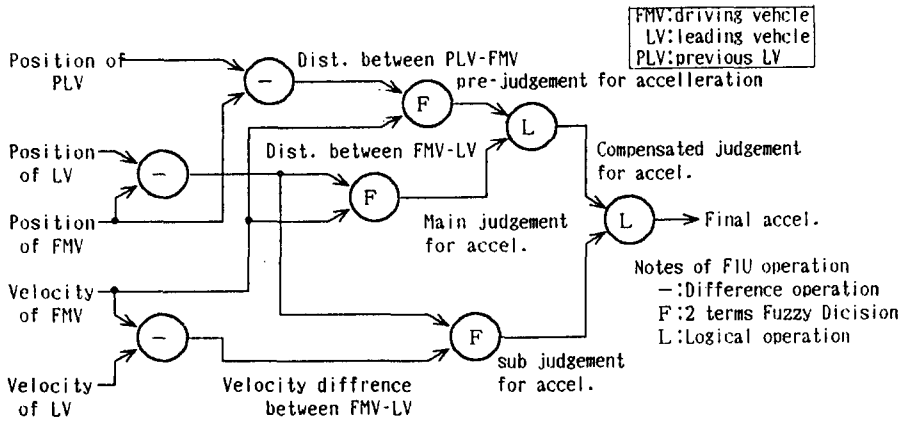

Fig.1 Multi-input fuzzy inference logic by cascaded 2 terms FIU

Consequently, memories for FIU will be unified with large capacity in whole. Fuzzy inference can be done in order of the leading step on the memory unified in whole. For this reason, the input data from outside to each FIU and output data of each FIU are necessary to keep during the computation of FIU. The capacity of the memories keeping those data needs twice numbers of FIU because of input with two terms, and also because output side needs the same quantities as input side.

Fig.3 shows a block diagram of two terms cascaded fuzzy unit constructed from four memories; logic, logic configuration, input data and output data. A control logic for them is constructed by using binary logic LSI, except logics concerning with the memory.

By only this method, we cannot deal with one more transactions of fuzzy inference through one sweep of FIU. In the simulation, it is necessary to deal with several thousands of transactions at a time. In such application that fuzzy inference mechanism is the same processing for all the transactions as FMV, a single cascaded FIU be possible to deal with hundreds of operations of fuzzy inference in FMV at a time, by increasing input and output memories corresponding to numbers of transactions and controlling to sweep FIU's logics from outside of FIU. The function to sweep this transaction and also the memory configuration and control of DRAM are included in the control LSI.

4. FUZZY PROCESSOR & ACCELERATOR

A circuit made of control LSI and memory at Fig.3 play merely a role of function of static logic. So, We need CPU to initialize an inner logical configuration and an inner table of FIU, and process input and output data for FIU.

Fig.4 shows a block diagram of fuzzy accelerator. We adopt 68302(6800) for CPU, and also serial interface and functions built in 68302 are used as data interface connecting to the routing switcher.

The membership functions and the value of fuzzy operation do not keep in the fuzzy processor itself. All of them is loaded down from the host computer. Moreover, fuzzy logics of each FIU are generated into memories as data on this CPU, and these data are loaded down to inference RAM at an initialization. The cascade logics are loaded down to configuration RAM from host computer, too. FIU is connected with two dual port RAMs to CPU.

They are input RAM and output RAM. The new information is prepared on input RAM at each time of sweeping of each transaction. And state of FMV in every sweep is set on input RAM. Information from output RAM is a few bytes on every FMV. Much data are necessary to be supplied to input RAM at every sweep to the contrary. This is a job of CPU. This information is usually set into output RAM at one sweep before. By changing dynamically the memory accessed, we can avoid the unusuful movement of data.

But as the construction to realize this method is hard, we don't adopt the method in our LSI. And we are under contemplation to connect another LSI in the outsides of FIU in the future. The host computer accesses to fuzzy accelerator through I/O interface. Every amount of information changed in road conditions(signal, generation of vehicles, existence of walkers and etc.) send to its accelerator. On the other hand,

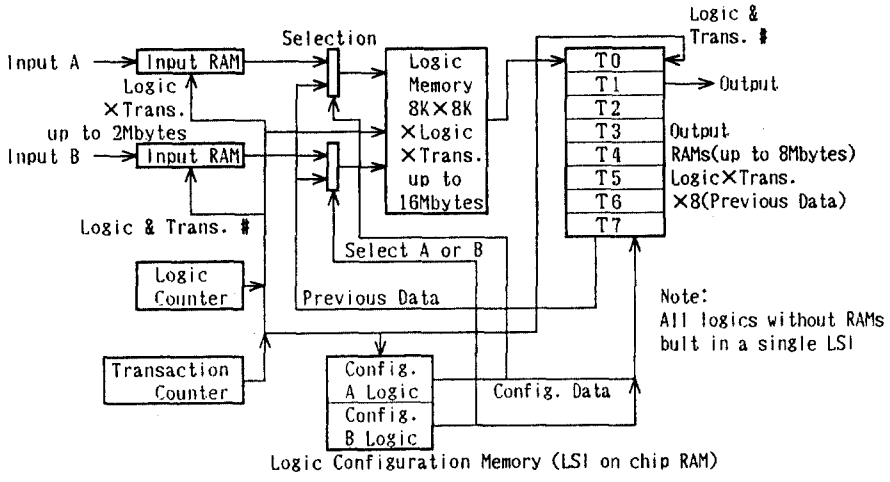

Fig.3 Functional block diagram of 2 terms fuzzy inference unit consisting of RAMs & controlling LSI

every situation of FMV(position, speed and etc.) are sent back to the host computer.

It is confirmed that the data transmission rate is a degree of 500 K bytes per second for carrying out a real time simulation of 1,000 FMVs at interval-scanning time 0.1 second. So, we adopted SCSI as the interface. Routing switcher has two functions; one is to distribute data received from host computer to each fuzzy processor, and the others is to transfer like cross switching from one fuzzy processor to the other. These processes are not fuzzilized. Transmission routes of these data are made of hardware and adopted serial interface for data connection to fuzzy processor.

5. CONCLUSION

We proposed a new hardware processor to simulate our FMV's fuzzy decision mechanism in MITRAM. We designed the processor, and also made a pilot breadboard of it to verify its functions and performance and carried out successfully several simulations by the breadboard. On the other hand, we carried out several simulations on a region with 71FIUs and 30FMVs to verify the mechanism of hardware processor by a personal computer, too.

As the results of them, it becomes clear that the execution time of the hardware processor has 12,500 times faster than one of a conditional computer, and furthermore the fuzzy inference of FMV be able to judge correctly the decision-making of driving such as stopping and starting of a vehicle and flattering driving even at a junction.

6. REFERENCE

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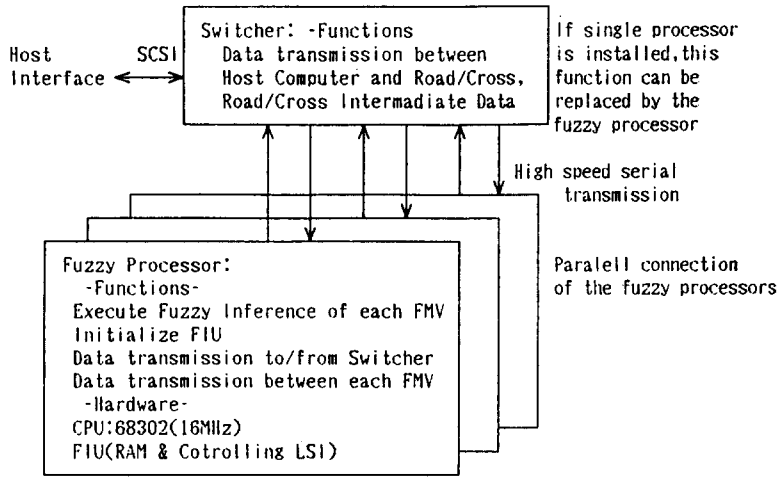

Fig.4 Block diagram of the fuzzy accellerator