Influence of Parasitic Parameters on Switching Characteristics and Layout Design Considerations of SiC MOSFETs

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Abstract

Parasitic parameters have a larger influence on Silicon Carbide (SiC) devices with an increase of the switching frequency. This limits full utilization of the performance advantages of the low switching losses in high frequency applications. By combining a theoretical analysis with an experimental parametric study, a mathematic model considering the parasitic inductance and parasitic capacitance is developed for the basic switching circuit of a SiC MOSFET. The main factors affecting the switching characteristics are explored. Moreover, a fast-switching double pulse test platform is built to measure the individual influences of each parasitic parameter on the switching characteristics. In addition, guidelines are revealed through experimental results. Due to the limits of the practical layout in the high-speed switching circuits of SiC devices, the matching relations are developed and an optimized layout design method for the parasitic inductance is proposed under a constant length of the switching loop. The design criteria are concluded based on the impact of the parasitic parameters. This provides guidelines for layout design considerations of SiC-based high-speed switching circuits.

Key words: Layout design, Parasitic capacitance, Parasitic inductance, Silicon Carbide (SiC)

I. INTRODUCTION

When compared with Silicon (Si) based power electronic devices, Silicon Carbide (SiC) materials have a wider band gap, higher electron mobility and higher thermal conductivity. As a result, SiC MOSFETs have a lower resistance, higher blocking voltage and junction temperature, and they have no current trails when compared with Si IGBT. This can reduce the switching losses, improve the switching speed and significantly improve the performance of power electronic converters. A high switching frequency is one of the most important directions in terms of application research for SiC devices [1], [2]. With an increase of the switching frequency, the influences of the parasitic parameters on the dynamic switching process of a device becomes more serious, resulting in oscillations in the switching transient and increasing the device stress and electromagnetic interference (EMI). Thus, it cannot give full play to the performance advantages of low switching losses under a high switching speed for SiC devices [3].

In recent years, many scholars have studied the influences of circuit parasitic parameters on the switching characteristics of SiC devices. Most of the research methods are divided into the following three types. For the first type, the parasitic parameters are considered as a network. The parasitic parameters of the circuit or power module are extracted, and the influences of parasitic parameters are simulated by modeling and simulation. The influences of each part of the parasitic parameters have not been studied [4], [5]. For the second type, a theoretical analysis is made on the influence of the parasitic parameters of each part. However, the nonlinearity of the switching device and the parasitic parameters of the actual circuit lead to a relatively high order for the model. For ease analysis, some approximations and assumptions are required.
The theoretical analysis results are usually complex, and the influences of the parasitic parameters cannot be directly derived from the expression. Moreover, the lack of experimental verification is also an unavoidable problem. Thus, theoretical analysis is of little use for the actual circuit design [6]. For the third type, the experimental method is used to test the effect of the parasitic parameters on the switching characteristics. However, the actual layout limitation is not taken into consideration when setting the value of the parasitic inductance. Only the influence of a single parasitic inductance is studied. The results are still not enough to support appropriate layout designs of the switching circuit for SiC devices [7].

Considering that the accuracy of SiC device modeling is affected by the parasitic parameters of the circuit, it is difficult to get close to real results by theoretically analyzing. Therefore, in this paper, the method of combining a theoretical qualitative analysis with experimental quantitative research is proposed. First, a mathematical model of a SiC MOSFET based a switching circuit considering parasitic parameters is established. The main factors affecting the switching characteristics are confirmed. Then a SiC MOSFET based high-speed double pulse test platform is set up and the influences of the parasitic parameters on the switching performance of the SiC devices is studied. Based on the concept of the current loop, the parasitic inductance of each part is classified into three categories, the main circuit parasitic inductance \( L_D \), the gate circuit parasitic inductance \( L_G \) and the common source parasitic inductance \( L_S \). In addition, the parasitic capacitances are classified into four categories, the gate-source capacitance \( C_{GS} \), the gate-drain capacitance \( C_{GD} \), and the drain-source parasitic capacitances \( C_{DS} \) and \( C_J \). Combined with the actual circuit layout, the parasitic capacitances, rather than the wire itself [8].

II. MODELING AND ANALYSIS OF SiC MOSFET SWITCHING CHARACTERISTICS

A principle diagram of the SiC MOSFET double pulse test circuit with parasitic parameters is shown in Fig. 1. Q is the SiC MOSFET. \( C_{GS} \), \( C_{GD} \) and \( C_{DS} \) are the gate-source, gate-drain and drain-source parasitic capacitances, respectively. \( C_J \) is the parasitic capacitance of the freewheeling diode \( D1 \). \( L_G \) is the parasitic inductance between the gate drive circuit and the gate pin, \( L_S \) is the parasitic inductance between the source pin and the gate drive circuit, and \( L_D \) is the load inductor. The parasitic inductance in the main circuit includes the distribution inductance of the drain pin \( L_{d1} \), the parasitic inductance of the diode \( L_{d1} \), and the PCB route parasitic inductances \( L_{d2} \) and \( L_{g2} \). \( R_i \) and \( R_G \) are the internal gate parasitic resistance and external drive resistance of the SiC MOSFET. By Faraday's law of electromagnetic induction, it is known that a closed current loop formed by wires produces parasitic inductances, rather than the wire itself [8]. According to this concept, it is possible to simplify the inductance of the main circuit. The parasitic inductance of the main power circuit loop is \( L_{G}=L_{d1}+L_{d2}+L_{a1} \). Thus, the parasitic inductance is classified into three categories, the parasitic inductance of the main power circuit loop \( L_D \), the gate circuit parasitic inductance \( L_G \) and the common source parasitic inductance \( L_S \). The induced voltage caused by the parasitic inductance \( L_G \) is obtained by Equ. (1) [7].

\[
L_G \cdot \frac{di_G}{dt} < \Delta U_{(\max)}
\]

Where \( \Delta U_{(\max)} \) is the maximum allowable gate oscillation peak voltage. The maximum allowable drain peak current caused by the gate voltage spike is limited by (2).

\[
g_{fs} \cdot \Delta U_{(\max)} < 10\% \cdot I_N
\]

Where \( g_{fs} \) is the transconductance and \( I_N \) is the rated current. Therefore, the gate circuit parasitic inductance \( L_G \) can be simplified as follows:

\[
L_G \cdot \frac{di_G}{dt} < \frac{10\% \cdot I_N}{g_{fs}}
\]
The second-order differential equation of the gate source voltage $u_{GS}(t)$ is obtained as Equ. (7) by combining Equ. (5) and Equ. (6).

$$U_g = R_g C_{GS} \frac{du_{GS}(t)}{dt} + \frac{du_{GS}(t)}{dt} + u_{GS}(t)$$

(7)

Applying a Laplace transform and solving the differential equation, the subsection expression of $u_{GS}(t)$ is expressed by following equations:

$$u_{GS}(t) = \begin{cases} 
U_{GH(1)} - U_{GH(2)} e^{\frac{t}{T_1}} \left( \cos \alpha_1 + \frac{\sin \alpha_1}{\alpha_1} \right), & 4y_1 \geq y_2^2 \\
U_{GH(1)} - U_{GH(2)} \left[ T_1 e^{\frac{t}{T_1}} - T_2 e^{\frac{t}{T_2}} \right], & 4y_1 < y_2^2
\end{cases}$$

(8)

$$U_{GH(1)} = U_{GH1} - U_{TH}, \quad U_{GH(2)} = U_{GH1} - U_{TH}$$

(9)

Where $y_1 = R_0 C_{GS} g_6 (L_D + L_S), \quad y_2 = R_0 C_{GS} C_{Gd} + L_S g_6, \quad T_1 = \frac{2y_1}{y_2}, \quad T_2 = \frac{2y_1}{y_2 + \sqrt{y_2^2 - 4y_1}}, \quad T_3 = \frac{2y_1}{y_2 - \sqrt{y_2^2 - 4y_1}}$

$$\alpha_1 = \frac{4y_1 y_2^2}{4y_1^2}$$

The initial conditions of the equations are $U_{GH(1)} = U_{GH1}, \quad U_{GH(2)} = U_{GH1} - U_{TH}$ for the turn-on transient, and $U_{GH(1)} = U_{GH1}, \quad U_{GH(2)} = -(U_{GH1} + U_{TH})$ for the turn-off. $U_{GH1}$ and $U_{GH2}$ are the positive voltage and negative voltage provided by the gate drive circuit, respectively. Combining the solution of $u_{GS}(t)$ with Equ. (4) and Equ. (5), the solution of the drain current and drain source voltage can be obtained. However, the solution of the gate source voltage depends on the initial conditions and parameters of the driving circuit. Therefore, it is difficult for the theoretical analysis results to show the influence of the parasitic inductance on the switching characteristics. In the limit cases, if $4y_1 \gg y_2^2$, the gate source voltage can be simplified as:

$$u_{GS}(t) \approx U_{GH(1)} - U_{GH(2)} \cos \frac{1}{y_1^2} t$$

(10)

The change rate of the leakage current is given by:

$$\frac{dI_L(t)}{dt} = -\frac{g_6 U_{TH} + I_s}{R_g C_{GS} g_6 (L_D + L_S)}$$

(11)

The overshoot of the turn-off voltage oscillation is given by:

$$\Delta U_{off} \approx \frac{2I_s (U_{TH} + I_s / g_6)}{R_g} \sqrt{\frac{L_D + L_S}{C_{Gd}}}$$

(12)

If $4y_1 \ll y_2^2$, the gate source voltage can be simplified as:

$$u_{GS}(t) \approx U_{GH(1)} - U_{GH(2)} e^{\frac{t}{y_1^2}}$$

(13)

The overshoot of the turn-off voltage oscillation is given by:
\[ \Delta U_{\text{off}} \approx (U_{\text{TH}} + I_L/g_{\text{fs}}) \cdot \frac{g_{\text{fs}}(L_D + L_S)}{R_0 C_{GD} + g_{\text{fs}}L_S} \] (14)

From the above discussions, it can be known that the switching characteristics are mainly influenced by the drain and source parasitic inductances \( L_D \) and \( L_S \), as well as the gate-drain capacitance \( C_{GD} \) and the gate-source capacitance \( C_{GS} \). With an increase of the parasitic inductance \( (L_D + L_S) \), the change rate of the drain current decreases, and the peak voltage of the turn-off transient increases. In the extreme case when \( 4y_1 << y_2 \), with an increase of the parasitic inductance \( L_S \) when the influence of \( g_{\text{fs}}L_S \) is in a dominant position, the peak voltage of the turn-off transient decreases. However, when \( L_S \) keeps increasing, the importance of \( g_{\text{fs}}L_S \) decreases. Therefore, the peak voltage of the turn-off transient becomes nearly constant.

### III. INFLUENCE OF PARASITIC INDUCTANCE ON THE SWITCHING CHARACTERISTICS

In order to quantify the influence of the parasitic inductance on the switching process, a double pulse circuit test platform was built. Fig. 3(a) and Fig. 3(b) show the schematic and prototype. The device under test is a 1200V/35A SiC MOSFET SCH2080KE from ROHM Co. The diode \( D_H \) is a SiC Schottky Barrier Diode (SBD) SCS210KG to reduce the influence of the reverse recovery current and to suppress the leakage current spikes caused by the diode. When the SiC MOSFET is switched on, the charge current generated by the equivalent parallel capacitance and the junction capacitance of the diode cause spikes in the drain current, which affects the accuracy of the test results. Therefore, a single-turn winding is used to reduce the equivalent parasitic capacitance. Voltage and current waveforms of the power device are measured by a high voltage differential probe (P5201) and a high frequency current probe (TCP2020) from Tektronix Co. The P5201 is connected directly to the gate and source of \( Q \). The TCP2020 detects the drain current of \( Q \) by a piece of yellow wire as shown in Fig. 3(b). The oscilloscope used is a Tektronix DPO3034, and the switching conditions are as follows: \( U_{\text{DC}} = 600V, L = 180\mu H \), the positive driving voltage is set to +18V, and the negative driving voltage is set to –2.6V. The total pulse time for the two pulses is \( \Delta t_p = 5\mu s \), and the maximum inductance current is \( I_{L_{\text{max}}} = 17A \) when \( U_{\text{DC}} = 600V \).

#### A. The Influence of the Gate Parasitic Inductance \( L_G \)

In order to analyze the influence of parasitic inductance on switching characteristics, small inductors were fabricated to simulate parasitic inductance. The test values of the four kinds of small inductors were 25nH, 50nH, 79nH and 95nH. The small inductors were connected between the gate pin and the drive circuit. Fig. 4 shows waveforms of the gate-source voltage \( u_{GS} \), drain-source voltage \( u_{DS} \) and drain current \( i_D \) with different gate parasitic inductances \( L_G \). The gate parasitic inductance \( L_G \) was resonant with the input capacitance \( C_{iss} = C_{GS} + C_{GD} \) (the damping coefficient \( \xi = \frac{R}{2} \frac{C_{iss}}{L_G} \)), causing an oscillation in the waveforms of the gate source voltage \( u_{GS} \). With an increase of \( L_G \), the amplitude of the
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oscillation in $u_{GS}$ increases as well. This phenomenon is particularly obvious in the turn-off waveform. However, the effects of $L_G$ on $u_{DS}$ and $i_D$ are not obvious. When $L_G$ increased from 25nH to 95nH, the waveforms of $u_{GS}$ and $i_D$ during the turn-on transient almost stay the same. For the turn-off transient, the overshoot voltage of $u_{GS}$ only increased from 630V to 650V.

From the above discussion, it can be known that $L_G$ has a great influence on the gate circuit. However, it has little influence on the power circuit. The main purpose of reducing $L_G$ is to avoid the large gate-source voltage spikes or the shoot-through caused by erroneous triggering of switches during the turn-off transient. Due to the fact that the design of the driving circuit guaranteed a very small gate parasitic inductance, the influence on the power circuit has been limited. It further illustrates the practical feasibility of the theoretical derivation while ignoring $L_G$ in Fig. 2.

B. The Influence of the Drain Parasitic Inductance $L_D$

In high speed switching processes, the change rate of the drain current ($di/dt$) is very high, and the induction electromotive force is induced on the drain parasitic inductance. The direction of the induced electromotive force is opposite that of the bus voltage during a turn-on transient. Therefore, the drain source voltage is reduced by $U_{LD}=L_D \cdot di/dt$. The direction of the induced electromotive force is the same as that of the bus voltage during a turn-off transient, which is superimposed on the drain-source voltage of the switches and causes voltage spikes. In addition, during a switching transient, the power circuit parasitic inductance $L_D$ is resonant with the output capacitance $C_{oss}(=C_{GD}+C_{DS})$ of the SiC MOSFET, the junction capacitance of the diode and the parasitic capacitance of the inductor. Furthermore, the oscillation can be coupled with the gate circuit by the Miller capacitance, causing oscillations on $u_{DS}$, $u_{GS}$ and $i_D$. The drain parasitic inductance is simulated by small inductances of 25nH, 50nH, 79nH and 90nH connected to the drain of the SiC MOSFET.

Fig. 5 shows waveforms of the gate-source voltage $u_{GS}$, drain-source voltage $u_{DS}$ and drain current $i_D$ with different drain parasitic inductances $L_D$. With an increase of $L_D$, the amplitude of the oscillation for $i_D$ increases. However, $u_{DS}$ is essentially unchanged during turn-on transients. In addition, during a turn-off transient, the amplitudes of the oscillations for both $i_D$ and $u_{DS}$ increase, as well as the turn-off energy.

C. The Influence of the Source Parasitic Inductance $L_S$

The change rate of the source current $di/dt$ during high speed switching induces an electromotive force in the opposite direction to the driving voltage. Therefore, the amplitudes of the driving voltage for turn-on and turn-off transients are reduced, which slows down the switching speed. It also causes negative feedback between the main circuit and the drive circuit. The source parasitic inductance is simulated by small inductances of 25nH, 50nH, 79nH and 90nH connected to the source of the SiC MOSFET. Fig. 6 shows waveforms of the gate-source voltage $u_{GS}$, the drain-source voltage $u_{DS}$ and the drain current $i_D$ with different source parasitic inductances $L_S$. As shown in Fig. 6, $L_S$ has an obvious effect and causes a significant delay on the turn-on and turn-off times.
Fig. 7. Relationship curve of voltage and current overshoot versus parasitic inductance: (a) Overshoot of $u_{DS}$ during turn-on transients; (b) Overshoot of $i_D$ during turn-on transients.

Fig. 8. Relationship curves of the turn-on and turn-off times versus the parasitic inductance: (a) Turn-on time; (b) Turn-off time.

Fig. 9. Relationship curves of the turn-on and turn-off energy losses versus the parasitic inductance: (a) Turn-on energy; (b) Turn-off energy; (c) Total switching energy.

D. Quantitative Analysis of the Influence of Parasitic Inductance

1) The Influence on the Voltage and Current Overshoot:

In order to compare the influences of different parasitic inductances on the switching characteristics, the relationships between the voltage and current overshoot with different values of $L_G$, $L_D$ and $L_S$ are given in Fig. 7. Consistent with the foregoing analysis, the effects of $L_G$ on $u_{DS}$ and $i_D$ are not obvious. With an increase of $L_G$, the amplitude of the oscillation of $u_{DS}$ and $i_D$ stays nearly the same. However, $L_D$ and $L_S$ have a significant influence on $u_{DS}$ and $i_D$. As shown in Equ. (13), the overshoot of the turn-off voltage oscillation is related to three parasitic parameters: $C_{GD}$, $L_D$ and $L_S$. For the parasitic inductance, when $L_D$ is increased, $\Delta U_{off}$ increases. When $L_S$ is increased, $\Delta U_{off}$ decreases. The experimental results are in good agreement with the theoretical analysis, as shown in Fig. 7(b). The turn-off overshoot increases with an increase of $L_D$ and decreases with an increase of $L_S$. The negative feedback effect caused by $L_S$ in the drive circuit has a suppressing effect on the oscillation caused by $L_D$.

2) The Influence on the Switching Time:

Fig. 8 shows the impacts of $L_G$, $L_D$ and $L_S$ on the turn-on and turn-off times. As shown in Equ. (14), $u_{GS}$ is mainly determined by $C_{GS}$, $C_{GD}$ and $L_S$, while $L_G$ and $L_D$ have almost no influence on $u_{GS}$. With an increase of $L_S$, the turn-on and turn-off times are significantly increased. As can be seen in Fig. 8, the impacts of $L_G$ and $L_D$ on switching time are not obvious.

3) The Influence on the Turn-On and Turn-Off Energy:

Fig. 9 shows the relationship between the switching energy losses and the parasitic inductance. With an increase of $L_G$, the turn-on and turn-off energy barely changes. With an
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increase of $L_D$, the turn-on and turn-off energy slightly decrease. Due to negative feedback, $L_S$ has a great influence on the switching energy. When $L_S$ is 95nH, the total switching energy is about 3 times $L_D$ with the same inductance.

From the above analysis, it can be seen that in the case of high speed switching, the gate parasitic inductance $L_G$ has a great influence on oscillations in the gate circuit. However, it has little influence in the power circuit. The drain parasitic inductance $L_D$ has a great influence on the current spikes and turn-off voltage spikes. It also has a certain effect on the oscillation of the waveform. A negative feedback effect is formed between the main circuit and the gate circuit through the source parasitic inductance $L_S$, which can restrain the oscillation and voltage spike caused by $L_D$. However, it also reduces the change rate of the drain current, which significantly affects the switching speed and switching energy.

**IV. OPTIMIZED LAYOUT DESIGN METHOD OF THE PARASITIC INDUCTANCE**

In high-speed switching drive circuits, the layout of the drive circuit and the main power circuit needs to be more compact. However, the PCB routes are limited by the actual layout. Therefore, it is difficult to take account of all the parasitic inductance at the same time. Due to the high priority of a compact layout, the total length of the loop routes is limited. Therefore, a comprehensive consideration between $L_S$ and $L_D$ is needed. Thus, the characteristics of the switching circuit can be optimized to meet the system performance requirements. In the experiments, four different combinations of $L_D$ and $L_S$ are selected (see in Table I) while keeping the sum of $L_D$ and $L_S$ almost unchanged.

Fig. 10 shows switching waveforms with different combinations of $L_D$ and $L_S$. The relationship between $di_D/dt$ and $L_S$ during a switching transient is shown in Fig. 11 with a constant sum of $L_D$ and $L_S$. During the turn-on process, the rising speed of $u_{GS}$ is reduced with an increase of $L_S$, a rising speed of $i_D$ and a falling speed of $u_{DS}$. As a result, the turn-on speed of the SiC MOSFET is reduced. Therefore, the energy of turn-on transient increases with an increase of $L_S$ as shown in Fig. 12.

In the turn-off process, when the sum of $L_D$ and $L_S$ is constant, with an increase of $L_S$, the falling speed of $u_{GS}$ is also decreased. Therefore, the falling speed of $i_D$ and the rising speed of $u_{DS}$ are reduced and the turn-off speed is reduced, as shown in Fig. 11(b). These experimental results also verify Equ. (14). Since $L_D + L_S$ stays constant, the turn-off voltage overshoot is determined by $L_S$. With an increase of $L_S$, the turn-off energy increases. However, the voltage spike in turn-off transients decreases. The overshoot of $u_{DS}$ during a turn-off transient and the overshoot of $i_D$ during a turn-on transient are given in Fig. 13 with different combinations of $L_D$ and $L_S$. With an increase of $L_S$, the overshoots of $u_{DS}$ and $i_D$ are reduced.

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**TABLE I DIFFERENT COMBINATIONS OF $L_D$ AND $L_S$**

![Fig. 10. Switching waveforms of $u_{GS}$, $i_D$ and $u_{DS}$ under different values of $L_S$ (under a constant sum of $L_D$ and $L_S$): (a) Turn-on waveforms; (b) Turn-off waveforms.](image)

![Fig. 11. Relationship curve of the switching speed under different values of $L_S$ (under a constant sum of $L_D$ and $L_S$): (a) Turn-on speed; (b) Turn-off speed.](image)
Fig. 12. Comparison of the switching energy under different values of $L_S$ (under a constant sum of $L_D$ and $L_S$).

Fig. 13. Relationship curves of voltage and current overshoots under different values of $L_S$ (under a constant sum of $L_D$ and $L_S$): (a) Overshoot of $u_{DS}$ during a turn-off transient; (b) Overshoot of $i_D$ during a turn-on transient.

From the above experimental results analysis, it can be seen that when the layout has been limited by actual factors and the sum of $L_D$ and $L_S$ cannot be further reduced, the distribution of $L_D$ and $L_S$ should be carefully considered to meet the requirements of the actual circuit. The basic laws are as follows. (1) If $L_S$ increases and $L_D$ decreases, the voltage spike in a turn-off transient and the current spike in a turn-on transient significantly decrease. However, due to the negative effect of $L_S$, the switching time increases, resulting in a significant increase in the switching energy loss. (2) If $L_D$ increases and $L_S$ decreases, the switching energy is reduced. However, this also increases the voltage spike in a turn-off transient and the current spike in a turn-on transient, which increases the voltage and current stresses of the SiC MOSFET.

Therefore, when the PCB layout is limited by physical constraints, it is necessary to optimize the design according to the requirements. If the purpose is to reduce the voltage and current spike, reducing $L_S$ and increasing $L_D$ appropriately is a good choice. However, when a low switching energy loss is needed, it is helpful to reduce $L_D$ and increase $L_S$.

Fig. 14(a) and Fig. 14(b) show the top layer and bottom layer of the proposed layout design for a SiC MOSFET driver, respectively. Since $L_G$ influences the gate-source voltage spike, the length of the gate loop should be as short as possible. As shown in Fig. 14(a), the gate and source connectors are three pins in parallel, which can minimize $L_S$ and $L_G$ introduced by pins. $L_S$ plays a more important role in the switching characteristics when compared with $L_G$. Therefore, as shown in Fig. 14(b), in order to achieve a higher switching speed, the driver output area has been covered with copper connected to the source.

V. INFLUENCE OF PARASITIC CAPACITANCE ON THE SWITCHING CHARACTERISTICS

The capacitances of SiC MOSFETs have a significant influence on the waveforms during switching transients. There are three parasitic capacitances in a SiC MOSFET: the gate-source capacitance $C_{GS}$, the gate-drain capacitance $C_{GD}$ and the drain-source capacitance $C_{DS}$. In order to quantify the
Influence of the parasitic capacitances on the switching process, voltage and current waveforms of the power device are measured P5201 and TCP2020 just like in section IV. The switching conditions are the same as in section IV: $U_{DC}=600V$, $L=180\mu H$, the positive driving voltage is set to $+18V$, and the negative driving voltage is set to $-2.6V$. The

Fig. 15. Switching waveforms of $u_{GS}$, $u_{DS}$ and $i_D$ under different values of $C_{GS}$. (a) Turn-on waveforms; (b) Turn-off waveforms.

Fig. 16. Turn-on and turn-off times under different values of $C_{GS}$.

Fig. 17. Turn-on and turn-off energy under different values of $C_{GS}$.

total pulse time for the two pulses is $\Delta t_p=5\mu s$, and the maximum inductance current is $I_{L_{\text{max}}}=17A$ when $U_{DC}=600V$.

A. The Influence of the Gate-source Capacitance $C_{GS}$

Small capacitors are paralleled between electrodes to simulate the parasitic capacitance of a SiC MOSFET in order to analyze the influence of the parasitic capacitance on the switching characteristics. The test values of the four kinds of small capacitors are 2.2nF, 3.3nF, 6.8nF and 18.0nF. Fig. 15 shows waveforms of the gate-source voltage $u_{GS}$, drain-source voltage $u_{DS}$ and drain current $i_D$ with different gate-source parasitic capacitors $C_{GS}$. Because the gate-source parasitic capacitor $C_{GS}$ is a part of the input capacitance $C_{in}(=C_{GS}+C_{GD})$, it is resonant with the gate parasitic inductance (the damping coefficient $\zeta = \frac{R}{2 \sqrt{L_G C_{GS}}}$), causing an oscillation in the waveform of the drain current $i_D$. With an increase of $C_{GS}$, the amplitude of the oscillation in $i_D$ decreases. Moreover, $C_{GS}$ mainly determines the switching time before and after the Miller platform. However, it has little effect on the Miller platform. In a turn-on transient, with an increase of $C_{GS}$, the Miller platform is almost unchanged. Therefore, the $dv/dr$ of the drain-source voltage $u_{DS}$ stays almost the same. However, the rise time of $u_{GS}$ increases because the time constant is determined by $C_{GS}$. The $dv/dr$ of the drain current $i_D$ significantly decreases, causing an increase in the rise time for $i_D$ and a decrease in the oscillation and spike for $i_D$. With an increase of $C_{GS}$, the delay of $u_{DS}$ increases due to an additional demand in the gate charge. In a turn-off transient, when $C_{GS}$ is increased, the falling speed of $u_{GS}$ decreases. However, it has little effect on $u_{DS}$ and $i_D$. For a turn-on transient, when $C_{GS}$ is increased from 2.2nF to 18.0nF, the overshoot current of $i_D$ is decreased from 19A to 16.5A.

With an increase of $C_{GS}$, as shown in Fig. 16 and Fig. 17, the turn-on time $t_{on}$ and turn-off time $t_{off}$ of a SiC MOSFET are increased. In addition, the turn-on energy and turn-off energy are also increased. As shown in Fig. 18, the turn-on current spikes and turn-off voltage spikes are also slightly increased.
B. The Influence of the Gate-drain Capacitance \( C_{GD} \)

Because the value of the Miller capacitance \( C_{GD} \) is two orders of magnitude smaller than that of \( C_{GS} \), the influence on the switching waveform for \( C_{GD} \) can be ignored when compared with \( C_{GS} \). However, the Miller platform is largely determined by \( C_{GD} \). According to an analysis of the ideal switching process, the length of the Miller platform affects the falling speed during a turn-on transient and the rising speed during a turn-off transient for \( u_{DS} \). As shown in Fig. 19(a), in the turn-on time, with an increase of \( C_{GD} \), the falling rate of \( u_{DS} \) decreases. However, the rising rate of the drain current does not change. As shown in Fig. 19(b), in the turn-off time, with an increase of \( C_{GD} \), the length of the Miller platform is extended and the rising rate of \( u_{DS} \) is decreased. Since the drain current \( i_D \) does not decrease until \( u_{DS} \) rises to the DC bus voltage, \( i_D \) is delayed by an increase of \( C_{GD} \). However, the current rate \( \frac{d}{dt}i_D \) stays the same.

Due to the Miller effect, a small increase of \( C_{GD} \) can result in a significant increase of the turn-on and turn-off times, as well as a large increase in the turn-on and turn-off losses, as shown in Fig. 20 and Fig. 21. However, with an increase of \( C_{GD} \), as shown in Fig. 22, the turn-on current spikes and turn-off voltage spikes barely change since \( C_{GD} \) accounts for a small portion of \( C_{iss} \) when compared with \( C_{GS} \).

C. The Influence of the Drain-source Capacitance \( C_{DS} \)

The additional drain-source parasitic capacitance \( C_{DS} \) is simulated by paralleling capacitance between the drain and source pins. As shown in Fig. 23(a), in the turn-on time, with an increase of \( C_{GD} \) from 680pF to 1.5nF, the turn-on waveform stays almost the same. In addition, the \( \frac{du}{dt} \) for \( u_{DS} \) and the \( \frac{di}{dt} \) for \( i_D \) stay nearly the same. Furthermore, an increase of \( C_{GD} \) has nearly no effect on the oscillation. This is due to the fact that during turn-on transients, the oscillation is mostly determined by the series resonance with \( L_{DS} \), \( L_s \) and \( C_i \). As shown in Fig. 23(b), in the turn-off time, with an increase of \( C_{GD} \), the \( \frac{du}{dt} \) for \( u_{DS} \) decreases, and the oscillations for \( u_{DS} \) and \( i_D \) increase. This is due to the fact that during a turn-off transient, the main power circuit can be seen as having a series resonant between \( L_{DS} \), \( L_s \) and \( C_{OSS}(=C_{DS}+C_{GD}) \). With an increase of \( C_{DS} \), \( C_{OSS} \) increases and the resonant frequency decreases. However, the resonance amplitude significantly increases.

With an increase of \( C_{DS} \) from 680pF to 1.5nF, the turn-on time is almost unchanged while the turn-off time increases.
Influence of Parasitic Parameters on Switching Characteristics and ... 

Fig. 23. Switching waveforms of \( u_{GS} \), \( u_{DS} \) and \( i_D \) under different values of \( C_{DS} \): (a) Turn-on waveforms; (a) Turn-off waveforms.

Fig. 24. Turn-on and turn-off times under different values of \( C_{DS} \).

Fig. 25. Turn-on and turn-off energy under different values of \( C_{DS} \).

Fig. 26. Voltage overshoot for \( u_{DS} \) and current overshoot for \( i_D \) under different values of \( C_{DS} \).

from 20ns to 80ns, as shown in Fig. 24. Therefore, as shown in Fig. 25, the turn-on loss barely changes, while the turn off loss increases from about 60\( \mu \)J to 160\( \mu \)J. However, with an increase of \( C_{DS} \), as shown in Fig. 26, the turn-on current spikes slightly increases from 3.0A to 3.5A while the turn-off voltage overshoot decreases from 90V to 70V. Moreover, during turn-off transients, a significant oscillation appeared when \( i_D \) decreased to zero, and the amplitude of the oscillation increased a lot with an increase of \( C_{DS} \). This was due to the resonant caused by \( L_D \), \( L_S \) and \( C_{OSS} \).

D. The Influence of the Parasitic Capacitance \( C_J \)

\( C_J \) is the parasitic capacitance of the freewheeling diode \( D_1 \) and the inductor \( L_i \). \( C_J \) affects the switching speed, voltage spikes, current spikes and switching energy. The influences of different values of \( C_J \) on the switching process are showed in Fig. 27 and Fig. 28. Fig. 27 shows switching waveforms of \( u_{GS} \), \( u_{DS} \) and \( i_D \) under different values of \( C_J \). With an increase of \( C_J \), the peak current and the oscillation amplitude increase during turn-on transients. When the switch turns off, with an increase of \( C_J \), it needs to draw more current to discharge \( C_J \). Therefore, the \( d/dt \) of the drain current increases. In addition, with an increase of \( C_J \), the rising speed for \( u_{DS} \) slightly decreased. Fig. 28 indicates that with an increase of \( C_J \), the turn-on and turn-off times increased. Fig. 29 shows the turn-on and turn-off energy under different values of \( C_J \). With an increase of \( C_J \), the turn-on energy increased but the turn-off energy decreased. Fig. 30 shows the influence of \( C_J \) on the voltage overshoot during turn-off transients and the current overshoot during turn-on transients. The current overshoot increased while the voltage overshoot decreased with an increase of \( C_J \).

From the above analysis, it can be seen that in the case of high speed switching, the gate-source parasitic capacitance \( C_{GS} \) has a negative influence on the turn-on and turn-off times, and a slight influence on the current spikes and voltage spikes. The gate-drain parasitic capacitance \( C_{GD} \) has a large influence on the turn-on and turn-off times, but little influence on the current spikes and voltage spikes. The drain-source parasitic capacitance \( C_{DS} \) has a significant influence on the turn-off time, but little influence on the turn-on time. In addition, \( C_{DS} \) has a certain influence on the current spikes and voltage spikes.
spikes. An increase of the capacitance of the freewheeling diode and the inductor $C_J$ has a negative influence on the turn-on and turn-off times.

VI. CONCLUSION

In this paper, the effects of parasitic parameters on the switching processes of SiC MOSFETs are studied systematically, and the influences of parasitic parameters on the switching characteristics are obtained.

A well-considered design has already ensured the minimization of the parasitic inductance of the gate driver loop. Therefore, the influence of $L_G$ on the switching characteristics is relatively small. However, the influence of $L_D$ on oscillations and voltage spikes is significant. The source parasitic inductance $L_S$ has some inhibitory effect on oscillations and voltage spikes, but it increases the switching energy loss. Therefore, an improved layout design method is proposed. The considerations to determine the distribution between the parasitic inductance $L_S$ and $L_D$ while the sum of $L_S$ and $L_D$ remains unchanged are also discussed. By this method, the optimization of different switching characteristics under the condition of a limited physical distribution can be reached.

The influences of parasitic capacitances on switching characteristics are also studied experimentally. The parasitic capacitances $C_{GS}$ and $C_{GD}$ have a great influence on switching times. With an increase of $C_{GS}$ and $C_{GD}$, the turn-on and turn-off times are noticeably increased. While $C_J$ can slightly effect the switching times, $C_{DS}$ has nearly no effect on the turn-on time but a large effect on the turn-off time. As for oscillation, an increase of $C_{GS}$ restrain switching resonance. An increase of $C_{DS}$ and $C_J$ reduces the turn-off voltage overshoot but increase the turn-on current overshoot. The influence of $C_{GD}$ on the oscillation in a power loop can be ignored.

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REFERENCES


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