Analysis and Implementation of a New Single Switch, High Voltage Gain DC-DC Converter with a Wide CCM Operation Range and Reduced Components Voltage Stress

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Abstract

This paper presents a single switch, high step-up, non-isolated dc-dc converter suitable for renewable energy applications. The proposed converter is composed of a coupled inductor, a passive clamp circuit, a switched capacitor and voltage lift circuits. The passive clamp recovers the leakage inductance energy of the coupled inductor and limits the voltage spike on the switch. The configuration of the passive clamp and switched capacitor circuit increases the voltage gain. A wide continuous conduction mode (CCM) operation range, a low turn ratio for the coupled inductor, low voltage stress on the switch, switch turn on under almost zero current switching (ZCS), low voltage stress on the diodes, leakage inductance energy recovery, high efficiency and a high voltage gain without a large duty cycle are the benefits of this converter. The steady state operation of the converter in the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is discussed and analyzed. A 200W prototype converter with a 28V input and a 380V output voltage is implemented and tested to verify the theoretical analysis.

Key words: Coupled inductor, High step-up voltage gain, Single switch, Switched capacitor, Low voltage stress

I. INTRODUCTION

Environment pollution and the depletion of fossil fuels have pushed researchers to work on renewable energy sources, especially solar energy. The output voltage of solar panels is usually less than 50 volts. However, in order to inject power to the grid, the DC level must be stepped up to 380-400V DC for a full bridge inverter and 750-800V DC for a half bridge inverter. The series connection of photovoltaic (PV) panels is a solution to produce such high voltages. However, due to shading and panel mismatch, maximum power point tracking (MPPT) is not achieved which reduces the system efficiency. Moreover, in the case of panel failure, the entire panel set fails. For these reasons, paralleling PV panels is a better choice. On the other hand, in low power applications, it is possible to use only one panel. In such cases, a DC-DC boost converter is needed to increase the DC voltage of the PV panel. DC-DC boost converters are categorized into isolated and non-isolated types. The efficiency of isolated converters is less than that of non-isolated converters, since all of the input power is transmitted via magnetic coupling. Moreover, a large winding turn ratio of the transformer in an isolated converter increases the winding parasitic capacitors and transformer leakage inductance, which results in oscillations and increased losses and electromagnetic interference (EMI) noise.

The conventional boost converter is the simplest topology of this type of converter. However, the gain and efficiency of this converter is limited because of its high conduction and switching losses due to the reverse-recovery of the output diodes and the larger conduction losses due to the applied high voltage switch.

To increase the voltage gain of a boost converter various techniques have been introduced. The voltage gain of a three-level boost converter is almost same as that of a conventional boost converter, and the voltage stress on the switches and output diodes is half the output voltage. However, the reverse recovery of the output diodes is still a
problem. In cascade boost converters, the voltage gain is high and equal to the product of its stages. However, the second stage has high voltage stress on the switch and diode, which results in low efficiency, due to two stage power processing. In addition, using two magnetic cores and switches, and its instability issue are the disadvantages of this converter [1]. In quadratic boost converters [1], [2], the active switch of the first stage is replaced with a diode, which makes the circuit simpler. However, like cascade boost converters, on the second stage, the high voltage stress on the output diode and active switch is equal to the output voltage. The integration of a boost converter with another converter, such as flyback or SEPIC [1], [3], [4] has the following advantages: some of the elements such as the active switch or inductor are shared between two converters, both converter outputs are added together, and the boost converter section behaves like a clamping circuit. The switched capacitor [1] and voltage lift [5] techniques are appropriate for low power applications. Meanwhile, in high power applications, high transient current passes through the active switch which reduces efficiency. Using voltage multiplier cells in the boost converter [6]-[9] is suitable for moderate voltage gain applications, because for a high gain voltage, a high number of cells decreases efficiency. Using a switched inductor in a boost converter [10] is also not appropriate for high voltage gain and high power applications, because the conduction losses of the switched inductor diodes are high, and the voltage stress of the active switch and output diode is equal to the output voltage. In active network converters (ANC) [10], the diodes of the switched inductor are removed and an active switch is added. In this configuration, the voltage and current stress on the switches are reduced. However, the voltage gain is low and it needs two isolated gate pulses for its two switches. Three state switching cell (3SSC)-based converters [11] have a low input current ripple, where the current ripple frequency of the auto transformer and inductor is twice the switching frequency, which reduces the volume and weight of the magnetic elements. Due to the presence of an autotransformer with a unit turn ratio, there is good current sharing between the switches. Although these converters have a large number of component, they are suitable for high power applications.

In high step-up applications, boost converters with coupled-inductors are particularly important. There are three main advantage of these converters. 1) Their high voltage gain with a low operating duty cycle can be adjusted by a proper turn ratio of the coupled inductor. 2) Their switch voltage stress is low. Therefore, switches with a low $R_{ds(on)}$ and low conduction losses can be utilized. 3) Their secondary leakage inductance reduces the reverse recovery ringing of the output diode.

There are three disadvantage of converters with coupled inductors. 1) When the active switch is turned off, the stored energy in the leakage inductance causes a voltage spike across the switch. 2) Their input current ripple is high, especially with increments of the turn ratio. 3) Using a higher turn ratio to achieve a higher voltage gain causes higher parasitic winding capacitors and leakage inductance, which increase the losses and EMI noise.

To overcome the problem of leakage inductance energy, Resistor-Capacitor-Diode (RCD) snubber circuits, passive clamp circuits [12] and active clamp circuits [13] have been proposed. The RCD snubber suppresses switch voltage spikes. However, it wastes the leakage inductance energy in the RCD resistor, which reduces the efficiency. Unlike the RCD snubber, both active and passive clamp circuits recover the energy of the leakage inductance. In the active clamp circuit, the zero voltage switching (ZVS) conditions is provided for each of the switches, but at the cost of an additional switch with an isolated drive circuit, resulting in increased complexity of the converter. Passive clamp circuits have simpler structure and do not need additional switches. References [3], [14], [18], [20], [23], [25] employ output stacking techniques to directly transferred the leakage inductance energy of the coupled inductor to the output.

To achieve a high voltage gain, various technique have been applied on the coupled inductor. In [18], by using output stacking and a switched capacitor in the secondary of the coupled inductor, the winding number of the coupled inductor is decreased and the voltage gain and core utilization-factor is increased. The authors of [14] proposed a high voltage gain converter with a low input ripple current, which is suitable for high power applications. This converters uses two coupled inductors, interleaved switching, a voltage multiplier cell, output stacking and voltage lift techniques. The converter in [20] has less input current ripple and the same voltage gain when compared to the converter in [14]. However, it uses two inductors and one coupled inductor. The converter in [21] uses a coupled inductor and the switched-capacitor technique. In flyback mode when the switch is off, four capacitor are charged. In the forward mode when the switch is on, the capacitors, input source and secondary of the coupled inductor are in series and supply the load. However, the source current in this converter is discontinuous.

In [22] a passive clamp capacitor, which recycles the leakage inductance energy, in series with the secondary of the coupled-inductor charges a voltage-lift capacitor. This increases the voltage gain of the converter. Using the three-winding coupled-inductor in [25] offers a more flexible adjustment of the voltage conversion and less voltage stress on each diode. However, it is more complicated. In [26], using two coupled-inductors and a switched-capacitor cell, a high step-up Z-source converter was proposed. Compared with a boost converter, the Z-source converter has a higher voltage gain. The converter in [26] has a high voltage gain and voltage spike across the switch is clamped. However, the presence of a diode at the input and a high current section cause losses which decreases efficiency. The converter in
[27] has a three-winding coupled-inductor and an isolated-gate driver for the switch, which makes it complicated. The authors of [28] proposed a high step up converter using an active network, a three-winding coupled-inductor and a switched-capacitor cell. The active network reduces the voltage and current stress on the active switches and increases the voltage gain. This converter is complicated, due to the three-winding coupled-inductor and the two active switches with isolated gate drives.

The authors of [23], [24] proposed a cascade coupled inductor with a boost converter, which achieved a low input ripple current and a high voltage gain. However, like quadratic boost converters, due to the two power processing stages in the high current section, the efficiency is reduced. In addition, these converters use two magnetic cores which increase the volume.

In this paper a high voltage gain converter using a boost coupled inductor with a passive clamp circuit is proposed that utilizes the switched capacitor and the voltage lift technique to further increase the voltage gain. The configuration of the passive clamp and switched capacitor circuit increase the voltage gain. A high voltage gain without a large duty cycle, a high conversion ratio, a wide CCM operation, low voltage stress on the output diode, leakage inductance energy recovery and high efficiency are the benefits of this converter.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1 shows the circuit configuration of the proposed converter. The coupled inductor is shown with its equivalent circuit including an ideal transformer, the magnetizing inductance $L_m$ and the leakage inductance $L_{lk}$. $N_p$ and $N_s$ are the number of primary and secondary winding turns of an ideal transformer, respectively. $C_1$ is a clamp capacitor, $C_3$, $C_5$, $C_7$ are switched capacitors, $C_2$ is a voltage lift capacitor, and $C_o$ is an output capacitor. $D_1$ is a clamp diode, $D_o$ is the output diode and $D_2$, $D_3$, $D_4$, $D_5$ are blocking diodes. The semiconductor elements are assumed to be ideal. The coupling coefficient is represented by $k=L_m/(L_m+L_{lk})$, and $n=N_s/N_p$ is the ideal transformer turn ratio.

A. Continuous Conduction Mode (CCM) Operation

There are five operating modes in one switching cycle of the proposed converter. Fig. 2 represents theoretical waveforms of the proposed converter at the CCM operation.

1) Mode I [$t_0$-$t_1$]: Fig. 3(a)

Before $t_0$, the switch $S$ is off and the diodes $D_3$, $D_4$, $D_5$ are conducting. At $t_0$, the switch $S$ is turned on. The primary side current of the coupled inductor $i_{Lk}$ increases linearly until it reaches the magnetizing inductor current $i_{Lm}$ at $t_1$. During this time interval the difference between $i_{Lm}$ and $i_{Lk}$ ($i_{Lm} - i_{Lk}$) flows through the primary side of the ideal transformer $T_s$. The current of $T_s$’s secondary is equal to $n(i_{Lm} - i_{Lk})$ which decreases linearly until it reaches zero at $t_1$. The currents of $D_3$, $D_4$, $D_5$ decrease linearly and reach zero at $t_1$. Therefore, the reverse recovery problems of these diodes are alleviated. In addition, $S_1$ turns on under almost ZCS.

2) Mode II [$t_1$-$t_2$]: Fig. 3(b)

At $t_1$, $i_{Lk}$ is equal to $i_{Lm}$. Therefore, the magnetizing inductance $L_{m}$ begins to absorb energy from $V_{in}$. The current and voltage direction in the primary and secondary side of $T_s$ are reversed. Diodes $D_2$, $D_3$ begin to conduct. In this mode, the voltage lift capacitor $C_2$ is charged via the clamp capacitor $C_o$, the switched capacitor $C_3$ and the secondary side of $T_s$. Moreover, the switched capacitor $C_5$ is charged via the switched capacitor $C_7$ and the secondary side of $T_s$.
3) Mode III \([t_2-t_3]\): Fig. 3(c)
At \(t_2\), switch \(S\) is turned off. Diode \(D_1\) conducts and transfers the energy of the leakage inductance \(L_{lk}\) to the clamp capacitor \(C_1\). Therefore, the voltage of the switch clamps to \(V_{C1}\). In addition, a part of the magnetizing inductance energy is absorbed by this capacitor in the next mode, which is used to charge the capacitor \(C_2\). In this mode, \(i_{Lk}\) is greater than \(i_{Lm}\) and \(i_{Lk}-i_{Lm}\) flows through the primary side of \(T_1\). \(L_m\) still absorbs energy and the polarity of the \(T_1\) voltage has not changed yet. Therefore, the difference of \(C_1\) in series with the primary side of the \(T_1\) voltages and the input source voltage are imposed to \(L_{lk}\) and force \(i_{Lk}\) to decreases rapidly to \(i_{Lk}\) at \(t_3\). The currents of the \(T_1\) secondary side and the diodes \(D_2, D_3\) decline and reach zero at \(t_3\).

4) Mode IV \([t_3-t_4]\): Fig 3(d)
In this mode, the current of the leakage inductance \(i_{Lk}\) is less than the current of the magnetizing inductance \(i_{Lm}\). Therefore, the current direction and voltage polarity of the \(T_1\) primary and secondary are reversed. The diodes \(D_3, D_4, D_0\) conduct and their currents increase. In this mode, \(D_1\) still conducts and the reduction rate of its current is less than that of the previous mode, because the \(T_1\) voltage polarity is reversed. At \(t_4\), \(i_{Lk}\) reaches \(i_{D0}\) and the diode \(D_1\) turns off.

5) Mode V \([t_4-t_5]\): Fig. 3(e)
During this time interval, the energy of the magnetizing inductance \(L_{m}\), leakage inductance \(L_{lk}\) and input source \(V_{in}\) along with \(C_2\) and \(C_3\) is delivered to the load \(R\). In addition, the switched capacitors \(C_1, C_4\) are charged. In this mode \(C_1, C_3\) are discharged. This mode ends at \(t_5\) when \(S\) is turned on and the next switching period starts.

B. Discontinuous Conduction Mode (DCM) Operation

Since the leakage inductance is very small, its voltage drop can be neglected when compared to the voltage across \(L_{m}\). Therefore, the leakage inductance is ignored in these models.

Fig. 4 shows theoretical-waveforms during the three major operating modes in the DCM. Fig. 5 shows the current flow paths for these modes.

1) Mode I \([t_0-t_1]\): Fig. 4(a)
At \(t_0\), the switch \(S\) is turned on. The magnetizing inductance \(L_{m}\) absorbs energy from the source and its current increases linearly from zero. Simultaneously, the coupled inductor is in forward operation and transfers a part of the source \((V_{in})\) energy to the capacitors \(C_2\) and \(C_3\). This mode ends at \(t_1\) when \(S\) is turned off.

2) Mode II \([t_1-t_2]\): Fig. 4(b)
In this mode, \(S\) is off. The energy of \(L_{m}\) is transferred to the capacitors \(C_1, C_3, C_4, C_10\) and the load \(R\). The capacitors \(C_2\)
and $C_3$ are in series with the source and $L_m$, and give their energy to $C_o$ and the load $R$. This mode ends at $t=t_2$ when $L_m$ is discharged.

3) Mode III: $[t_2,t_3]$ Fig. 4(c)

In this mode, the switch $S$ remains off and the $L_m$ current is zero. Therefore, the load $R$ is supplied by $C_o$.

### III. Steady-State Analysis of the Proposed Converter

#### A. CCM Operation

Modes I and III are very short, and can be neglected in the calculation of the converter DC gain. In modes III and IV the energy of the leakage inductor $L_l$ is released to the clamp capacitor $C_l$. As shown in the appendix, the duty cycle of the charging clamp capacitor $C_l$, if mode III is neglected, is:

$$D_{c_1} = \frac{t_{c_1}}{T_s} = \frac{2(1-D)}{3n+2} \quad (1)$$

where $t_{c_1}$ is the charging duration of $C_l$, and $T_s$ is the switching period. Applying the voltage-second balance principle on $L_l$ and $L_m$ yields:

$$v_{l_k}^{IV} = \frac{D(3n+2)(1-k)}{2(1-D)} V_{in} \quad (2)$$

$$v_{l_m}^{IV,V} = \frac{DKV_{in}}{1-D} \quad (3)$$

where $k$ is the coupling-coefficient and it is equal to $k=L_m/(L_m+L_l)$.

By using (2), (3) the voltage of the clamp capacitor $C_l$ can be obtained as:

$$V_{c_1} = v_{l_k}^{IV} + v_{l_m}^{IV,V} + V_{in} = \frac{V_{in}}{1-D} + \frac{3nD(1-k)}{2(1-D)} \quad (4)$$

Using (3), the voltage across the switched capacitors $C_s,C_j$ can be written as:

$$V_{c_3} = V_{c_4} = V_s^V = nV_{l_m} = \frac{nDKV_{in}}{1-D} \quad (5)$$

Using (5), the voltages of the lifting capacitor $C_2$ and the switched capacitor $C_3$ are obtained as:

$$V_{c_2} = V_{c_1} + V_{c_3} + V_{s}^{II} = \left(\frac{1+nk}{1-D}\right) + \frac{3nD(1-k)}{2(1-D)}V_{in} \quad (6)$$

$$V_{c_5} = V_{c_4} + V_{s}^{II} = nk\left(1 + \frac{D}{1-D}\right)V_{in} \quad (7)$$

The output voltage $V_o$ is given as:

$$V_o = V_{in} + V_{l_m}^{IV} + V_{c_2} + V_{s}^{V} + V_{c_5} \quad (8)$$

Substituting (3),(4),(6) and (7) into (8) results in the DC voltage gain $M_{CCM}$ as:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{4(1+nk)-2D(1-k)+nD(3-k)}{2(1-D)} \quad (9)$$

Fig. 6 shows the voltage gain variations versus the duty ratio of the proposed converter, in the CCM operation for various coupling coefficient $k=1, 0.95$ and for $n=1.5, 2, 3, 4$. Fig. 6 concludes that the voltage gain is not sensitive to the coupling coefficient $k$. 

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Fig. 4. Theoretical waveforms of the proposed converter at the DCM operation.

Fig. 5. Current flowing path of operating modes during one switching cycle at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.
For $k=1$ the ideal CCM voltage is:

$$M_{CCM} = \frac{2(n+1)+nD}{1-D}$$

(10)

Fig. 7 shows variations of the CCM voltage gain versus the duty ratio of the proposed converter and the converters in [15]-[19] when $k=1$ and $n=2$.

The voltage stress of switch $S$ and diodes $D_{1}$, $D_{5}$, $D_{6}$, $D_{7}$, $D_{8}$, $D_{9}$, $D_{10}$ are:

$$V_{S} = \frac{V_{o}+nV_{in}}{3n+2}$$

(11)

$$V_{D1} = \frac{V_{o}+nV_{in}}{3n+2}$$

(12)

$$V_{D2} = V_{D0} = \frac{(n+1)(V_{o}+nV_{in})}{3n+2}$$

(13)

$$V_{D3} = V_{D4} = V_{D5} = \frac{n(V_{o}+nV_{in})}{3n+2}$$

(14)

**B. DCM Operation**

In the previous section, while neglecting the leakage inductance, three major operational modes are described. According to Fig. 4 in mode I, following equations can be written:

$$v_{Lm}^{I} = V_{in}$$

(15)

$$v_{S}^{I} = nV_{in}$$

(16)

$$I_{Lmp} = \frac{V_{in} DT_{S}}{L_{m}}$$

(17)

where $I_{Lmp}$ is the peak value of $L_{m}$. Applying volt-second balance principle to $L_{m}$ yields:

$$\int_{0}^{DT_{S}} v_{Lm}^{I} dt + \int_{0}^{(D+D_{1})T_{S}} v_{Lm}^{II} dt + \int_{(D+D_{1})T_{S}}^{T_{S}} v_{Lm}^{III} dt = 0$$

(18)

where $D_{1}$ is the duty cycle of the conducting diode $D_{1}$. Considering $v_{Lm}^{III} = 0$ and substituting (15) into (18) yields:

$$v_{Lm}^{II} = \frac{D}{D_{1}} V_{in}$$

(19)

Therefore, the secondary winding voltage in mode II is:

$$v_{s}^{II} = n v_{Lm}^{II} = \frac{nD}{D_{1}} V_{in}$$

(20)

According to Fig. 5(b) and using (19), (20) the following equations can be written:

$$V_{C1} = V_{in} + v_{Lm}^{II} = (1 + \frac{D}{D_{1}}) V_{in}$$

(21)

$$V_{C3} = V_{C4} = v_{S}^{II} = \frac{nD}{D_{1}} V_{in}$$

(22)

Writing the voltage equations for Fig. 5(a) and using (21), (22), $V_{C2}$ and $V_{C3}$ are obtained as:

$$V_{C2} = V_{C1} + V_{C3} + v_{S}^{I} = (n+1)(1 + \frac{D}{D_{1}}) V_{in}$$

(23)

$$V_{C5} = v_{S}^{I} + V_{C4} = n(1 + \frac{D}{D_{1}})$$

(24)

The output voltage is:

$$V_{o} = V_{in} + v_{Lm}^{II} + V_{C2} + v_{S}^{II} + V_{C5}$$

(25)

Substituting (19), (20), (23) and (24) into (25) yields:

$$V_{o} = [2(n+1) + \frac{D}{D_{1}} (3n + 2)]$$

(26)

Therefore:

$$D_{L} = \frac{(3n+2)DV_{in}}{V_{o} - 2(n+1)V_{in}}$$

(27)

As expressed in the Appendix, in the same way, in mode II the charges and conducting durations of $D_{1}$, $D_{3}$, $D_{5}$, $D_{6}$ are equal. Therefore, the $D_{0}$ peak current is:

$$i_{peak}^{D_{0}} = i_{peak}^{D_{1}} = i_{peak}^{D_{3}} = i_{peak}^{D_{4}} = \frac{I_{Lmp}}{3n+2}$$

(28)

Since the average current of $D_{0}$ is equal to the average current of the load:

$$\frac{1}{2} D_{L} i_{peak}^{D_{0}} = \frac{V_{o}}{R}$$

(29)

The normalized magnetizing inductor time constant is defined as:

$$\tau_{Lm} = \frac{L_{m}}{RT_{S}}$$

(30)

Equations (17),(27)-(30) yields the dc gain of the proposed converter in the DCM:

$$M_{DCM} = (n+1) + \sqrt{(n+1) + \frac{D^{2}}{2\tau_{Lm}}}$$

(31)
TABLE I

<table>
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<tr>
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<td>Voltage gain</td>
<td>( \frac{1+2n-nD}{1-D} )</td>
<td>( \frac{2+n-nD}{1-D} )</td>
<td>( \frac{1+2n-nD}{1-D} )</td>
<td>( \frac{1+2n-nD}{1-D} )</td>
<td>( \frac{2+3(n-1)}{1-D} )</td>
<td>( \frac{2(n+1)+nD}{1-D} )</td>
</tr>
<tr>
<td>Voltage stress on switch</td>
<td>( \frac{V_o-nV_{in}}{n+1} )</td>
<td>( \frac{V_o+nV_{in}}{2(n+1)} )</td>
<td>( \frac{V_o+nV_{in}}{(n+1)} )</td>
<td>( \frac{V_o-nV_{in}}{2(n+1)} )</td>
<td>( \frac{V_o-nV_{in}}{3n+2} )</td>
<td>( \frac{V_o+nV_{in}}{3n+2} )</td>
</tr>
<tr>
<td>The highest voltage stress on diodes</td>
<td>( \frac{n(V_o-nV_{in})}{n+1} )</td>
<td>2</td>
<td>( \frac{n(V_o+nV_{in})}{3n+1} )</td>
<td>( \frac{n(V_o-nV_{in})}{n+1} )</td>
<td>2</td>
<td>( \frac{n(V_o+nV_{in})}{3n+2} )</td>
</tr>
<tr>
<td>Series elements between switch and clamp capacitor</td>
<td>1 diode</td>
<td>1 diode and 1 capacitor</td>
<td>1 diode</td>
<td>1 diode</td>
<td>2 diodes and 1 capacitor</td>
<td>1 diode</td>
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<tr>
<td>Quantities of diodes</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>5</td>
<td>6</td>
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</table>

C. BCM Condition

In the boundary condition mode (BCM), the voltage gains of the CCM and DCM operations are equal. From (14), (31), the boundary normalized magnetizing-inductor time-constant can be expressed as:

\[
\tau_{Lmb} = \frac{1}{2} \frac{D^2}{(2nD+nD+1)(1-D)^2-(n+1)}
\]

(32)

The variation curve of \( \tau_{Lmb} \) versus the duty cycle \( D \), with \( n=2 \) for this converter and the converters of [15]-[19] are plotted in Fig. 8. For each converter, if \( \tau_{Lmb} \) is greater than \( \tau_{Lmb} \), that converter operates in the CCM. As this figure shows, the proposed converter has a wider CCM operational region than the converters presented in [15]-[19].

The comparison among the proposed converter and the converters in [15]-[19] are summarized in Table I. More series elements between the switch and the clamped capacitor increases the parasitic inductance and resistance, which results in a higher voltage spike across the switch.

IV. DESIGN GUIDELINES AND EXPERIMENTAL RESULTS

To verify the theoretical model, a prototype converter with the specifications in Table II is designed and implemented.

The first step of the design is selecting the nominal full load duty cycle. A larger duty-cycle results in a higher voltage stress. On the other hand, a lower duty-cycle results in a higher rms (root-mean-square) current and conduction losses. An appropriate duty cycle selection is considered as \( D=0.6 \). According to the input and output voltage of the converter, and using equation (10), the turns ratio \( n \) is obtained. In this example, assuming \( D=0.6 \) results in \( n=1.3 \). Since the winding turn numbers \( N_1 \) and \( N_2 \) are small, \( n=1.5 \) is
selected. Therefore, the theoretical duty cycle $D=0.57$ is yielded. In the next stage, the range of the converter CCM operation is selected, and by using (30) and (31), the value of $L_w$ is obtained. In this example, the range of the CCM operation is chosen as 25%-100% full load. Therefore, $L_w=83\mu H$ is yielded. The voltage stresses of the switch and diodes are obtained based on Equations (11)-(14). Equations (4)-(7) are used to obtain the voltage of the capacitors $C_f, C_v, C_s, C_r, C_b$. Since the charges absorbed or produced by the capacitors $C_f, C_v, C_s, C_r, C_b$ are all equal, the size of these capacitors are obtained as:

$$C_l = \frac{\Delta Q_l}{\Delta V_l} = \frac{I_0 T_s}{rV_l}$$

where $I_o$ is the load current, $T_s$ is the switching period, and $r$ is the ripple factor of the capacitor voltage, which is equal to the ratio of the capacitor peak-to-peak ripple voltage to the capacitor average voltage. $V_l$ is the average voltage of the capacitor. By choosing $r=.01$, the size of the capacitors are $C_f=10\mu F$, $C_v=6.4\mu F$, $C_s=C_r=18.7\mu F$, $C_b=10.4\mu F$. Table III and Fig. 9 show the component specifications and a photo of the implemented converter, respectively.

Fig. 10 presents experimental results obtained with the converter under full load conditions. These waveforms confirm the steady-state operating modes of the converter. Fig. 10(a) shows the leakage inductance current $i_{lb}$ and drain-source voltage of the switch $V_{ds}$, which shows that the peak voltage $V_{ds}$ is limited to 85V. Therefore, a MOSFET with a low withstand voltage and conduction losses can be used. Fig. 10(b) shows that the switch $S$ turns on under almost ZCS. Fig 10(c) shows the switch $S$ turn off interval, which is used to calculate switching turn off losses. Fig. 10(d) shows that after the switch turns off, the clamp diode $D_1$ starts to conduct and the leakage inductor energy is released to the capacitor $C_r$. The conduction time of $D_1$ is consistent with (1). Figs. 10(e)-(h) show that when the switch is on, $D_2$ and $D_3$ conduct and when it is off $D_1$ and $D_3$ conduct. Fig. 10(i) shows the input and output voltage of the converter. Fig. 11 shows the output voltage and output current when load steps up/down from $P_o=70W$ to a full load of $P_o=200W$.

Table IV presents the measured DC voltage of the capacitors $C_1$, $C_2$, $C_3$, $C_4$, $C_5$ in accordance with (4)-(7). These results show that the measured voltages of the capacitors are consistent with the theoretical calculations.

To estimate the efficiency of the converter under a full load, the conduction losses of the switch, diodes and coupled-inductor, as well as the turn on and turn off switching losses are estimated. Assuming that the initial efficiency is equal to 0.95, the RMS value of the input or switch current $I_{DS rms}$ is approximately equal to:

$$I_{DS-rms} = \frac{P_{in}}{\eta V_{in} \sqrt{D}} = \frac{200}{0.95 \times 28 \times \sqrt{0.57}} = 9.96A$$

The resistance of IRF4410 in the on-state is 9mΩ. The total copper resistance transferred to the primary of the coupled-inductor is 35mΩ. Therefore, the switch and inductor conduction losses $P_{cond_{sw}}, P_{cond_{cu}}$ are:

$$P_{sw} = R_{sw-on} \times (I_{sw-rms})^2 = 0.09 \times 9.96^2 = 0.89$$

$$P_{cu} = R_{cu} \times (I_{cu-rms})^2 = 0.035 \times 9.96^2 = 3.47W$$

The conduction losses of the diodes are almost equal to the multiplication of their average current and their forward voltage drop. The average current through the diodes $I_{diodes-avg}$ is equal to the load current. By considering $V_{D1} = 0.7V$, $V_{D2} = V_{D3} = 0.94V$ and $V_{D4} = V_{D5} = 1.15V$ from the diode datasheets, the diodes conduction losses $P_{cond_{diodes}}$ are:

$$I_{diodes-avg} = \frac{P_o}{V_o} = \frac{200}{380} = 0.526A$$

$$P_{cond_{diodes}} = \sum_{i=1}^{6} V_{f} I_{diode-avg}$$

$$= 0.526 \times (0.7 + 3 \times 0.94 + 2 \times 1.15)$$

$$= 3.06W$$

The turn-on switching losses are due to the discharge of the switch output capacitor ($C_{oss}$) during turn on, and the overlap of the switch voltage and current during a switching interval. According to the data sheet of an IRF4410, at $V_{DS}=68V$, the $C_{oss}$ discharged energy is 1µJ. Therefore, the switching turn on losses are:

$$P_{sw-on} = E_{oss} * f_{sw} = 1\mu J * 50kHz = 0.05W$$

Using Eq. 10(b), the second term due to the overlap is:

$$P_{overlap} = f_{sw} \int_{0}^{f_{sw}} I_{DS} \times V_{DS} \times dt = 0.5W$$

Therefore, the total switch turn-on losses are equal to:

$$P_{sw-on} = P_{sw-on} + P_{overlap} = 0.05 + 0.5 = 0.55W$$

According to Fig. 10(c), the turn off losses are:

$$P_{sw-off} = f_{sw} \int_{0}^{t_{on}} I_{DS} \times V_{DS} \times dt$$

$$= 50kHz \times \frac{1}{6} \times 10A \times 85V \times 80ns = 0.57W$$
Fig. 10. Experimental result of the converter under full load conditions.

Fig. 11. Load variation between $P_o=70$W and a full-load of $P_o=200$W.


<table>
<thead>
<tr>
<th>Parameter</th>
<th>Vc1</th>
<th>Vc2</th>
<th>Vc3</th>
<th>Vc4</th>
<th>Vc5</th>
<th>Vco</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured DC Voltage</td>
<td>68V</td>
<td>160V</td>
<td>57V</td>
<td>57V</td>
<td>95V</td>
<td>380V</td>
</tr>
<tr>
<td>Estimated DC Voltage</td>
<td>65V</td>
<td>163V</td>
<td>55V</td>
<td>55V</td>
<td>97V</td>
<td>380V</td>
</tr>
</tbody>
</table>

### Fig. 12. Measured efficiency under various output powers.

Therefore, the estimated efficiency at a full load is:

\[
\eta = \frac{P_o}{P_o + P_{losses}} = \frac{200}{200+8.54} = 95.9\% \quad (43)
\]

The measured efficiency of the proposed converter is shown in Fig. 12. The maximum efficiency is 96.1%, which occurs at an output-power of 80W. The full load efficiency is 94.7%. The difference between the estimated efficiency (95.9%) and the measured efficiency (94.7%) at a full load is due to the core losses and other losses.

## V. CONCLUSIONS

This paper proposed a new high step up DC-DC converter. By using a coupled inductor and utilizing the switched capacitor and voltage lift techniques, a high voltage gain is achieved. In this converter, the energy of the leakage inductance is recycled via a passive clamp circuit and the switch peak voltage is limited at 85V. Therefore, a MOSFET with a low withstand voltage and low conduction losses can be utilized. The steady-state operation of the converter in the CCM and the DCM is analyzed and the boundary condition is calculated. It is shown that the proposed converter has a high voltage gain and a wide CCM operation range with a low turn-ratio coupled inductor. A laboratory prototype is implemented in the laboratory. The prototype verifies the theoretical analysis. Finally an analysis of the losses is carried out and the experimental efficiency is obtained.

### APPENDIX: \(D_{c1}\) CALCULATION

\(D_{c1}\) is the conducting duty-cycle of the diode \(D_1\). To calculate \(D_{c1}\), the ripple of the magnetizing inductor current \(I_{Lm}\) is neglected. In modes III and IV, the leakage inductor energy is released to the clamp capacitor \(C_1\). Since the interval of \([t2-t3]\) is very short, it is neglected. In the \([t3-t4]\) interval, the \(D_{c1}\) current linearly decreases from \(I_{Lm}\) to zero. Therefore, the charge value of the capacitor \(C_1\) is:

\[
Q_{\text{charge}}^{c1} = \frac{1}{2} I_{Lm} D_{c1} T_s \quad (44)
\]

In steady-state operation, the charge balance principle yields:

\[
Q_{\text{charge}}^{c5} = Q_{\text{discharge}}^{c4} \quad (45)
\]

\[
Q_{\text{discharge}}^{c1} = Q_{\text{discharge}}^{c3} = Q_{\text{discharge}}^{c2} \quad (46)
\]

\[
Q_{\text{discharge}}^{c5} = Q_{\text{discharge}}^{c2} \quad (47)
\]

Thus, considering that the charging time of \(C_1\), \(C_4\) is equal to the discharging time of the capacitors \(C2\), \(C5\), the current of these the capacitors are equal:

\[
i_{\text{charge}}^{c3} = i_{\text{charge}}^{c4} = i_{\text{discharge}}^{c5} = i_{\text{discharge}}^{c2} \quad (48)
\]

Therefore, in the \([t3-t4]\) interval, the current of the capacitor \(C_2\) is equal to:

\[
i_{\text{discharge}}^{c2} = \frac{I_{Lm}}{3n+1} \quad (49)
\]

During the \([t1-t2]\) interval, the current of \(C_2\) increases from zero to \(I_{Lm}/(3n+1)\). Therefore, the total charge of \(C_2\) that discharges in the \([t1-t2]\) interval is equal to:

\[
Q_{\text{discharge}}^{c2} = \frac{I_{Lm}}{3n+1} (1 - D - D_{c1}) T_s + \frac{1}{2} \frac{I_{Lm}}{2n+1} D_{c1} T_s \quad (50)
\]

In steady-state operation, the charged and discharged charges of \(C_1\), \(C_2\) are equal \((Q_{\text{charge}} = Q_{\text{discharge}})\). Therefore, using (44), (46) and (50), \(D_{c1}\) is obtain as:

\[
D_{c1} = \frac{2(1-D)}{3n+2} \quad (51)
\]

### REFERENCES


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