Bidirectional Quasi-Cuk DC/DC Converter with Reduced Voltage Stress on Capacitor and Capability of Changing the Output Polarity

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Abstract – In this paper, a bidirectional topology for quasi-Cuk dc/dc converter with capability of zero-voltage and zero-current-switching (ZVZCS) is proposed. The bidirectional quasi-Cuk (BQ-Cuk) converter has different voltage and current transfer ratio, reduced voltage stress on capacitor and capability of changing the output polarity in comparison with conventional bidirectional Cuk converter. In this paper, steady-state analysis of the quasi-Cuk converter with capability of ZVZCS in turn-on is presented. Then, critical inductances for transient from this operation to two new operations are calculated. Next, besides values designing of used elements, maximum and minimum value of their current and voltage are calculated. Finally, experimental results to verify the accuracy of the proposed converter in different operating modes are presented.

Keywords: Critical inductances, Cuk converter, DC/DC converter, Change of output polarity

1. Introduction

The common types of dc/dc converters are buck, boost, buck-boost, Cuk [1], Sepic [2], and Zeta [3]. In spite of the many applications of the presented conventional converters in [1-3], these converters are not suitable for applications that bidirectional power flow management is needed. A kind of bidirectional topologies is bidirectional Cuk converter. For creating soft switching in the bidirectional Cuk (B-Cuk) converter, a bidirectional topology for this converter based on zero voltage switching (ZVS) has been presented in [4]. Although the presented topology can cause bidirectional power flow with the capability of soft switching, but the number of passive elements and active device increase, which causes an increase in size, weight and cost. In [5], a non-isolated topology for improving the voltage gain of conventional bidirectional buck-boost converter has been presented, but this topology has a higher number of switches than the conventional topologies. In [6], another topology with ZVS capability has been presented. This topology despite the advantages like proper voltage gain in boost and buck operating modes has various disadvantages such as increased number of active devices like switches and diodes. Also, employing another inductor beside mutual inductances causes an increase in circuit volume. In [7-9], topologies of dc-dc converters based on mutual inductances have been presented. The voltage transfer ratio in this topology depends on the mutual inductors winding turns ratio, which causes a restriction in achieving a desired voltage transfer ratio. In addition to this restriction, employing more switches causes an increase in cost and complexity in control of the converter.

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In this paper, based on presented concepts in [10] a bidirectional topology for quasi-Cuk dc/dc converter with capability of ZVZCS is proposed. One of the outstanding features of this converter is positive and negative voltages producing capability at the output. In the following sections, steady-state analysis of the bidirectional quasi-Cuk converter in different operating modes is investigated, and ZVZCS capability of switches in turn-on is shown. Then, voltage conversion ratio and voltage stress on capacitors are derived and comparison with the conventional counterpart demonstrates the outstanding features of the quasi-Cuk converter. Moreover, critical inductances are calculated, and the quasi-Cuk converter in two new operations is studied. Next, designing considerations of the converter is provided. Finally, experimental results to verify the correct operation of the topology in different operating modes are presented.

2. Bidirectional Quasi-Cuk Topology

Fig. 1 shows the power circuit of ZVZCS BQ-Cuk converter. According to this figure, inductors L_1 and L_2 , capacitors C_1 and C_2 , switch S_1 with anti-parallel diode D_1 and switch S_2 with anti-parallel diode D_2 associated with input source with voltage V_i and the output load with resistance R_L are constituting the elements of the converter.

Fig. 1. Power circuit of ZVZCS BQ-Cuk topology

When the BQ-Cuk converter has four operating modes, this operation is called SD operation. For simplicity, in analysis of the BQ-Cuk converter, all elements are considered ideal [11, 12].

First operating mode: In this operating mode and in the steady-state, S_1 , S_2 and D_2 are off, thus, the sum of the currents through L_1 and L_2 flows through the D_1 . Given to the fact that in this operating mode voltage across L_1 is negative and constant, therefore, current through inductor decreases linearly from its maximum value (I_{LP1}) and energy of that decreases. The currents through L_1 and L_2 (i_{L1} and i_{L2}) are calculated from the following equations:

$$i_{L1} = I_{LP1} + \frac{1}{L_1} \int_0^t (-V_i) dt = I_{LP1} - \frac{V_i}{L_1} t \quad (1)$$

$$i_{L2} = i_{C1} = I_{LP2} + \frac{1}{L_2} \int_0^t (-V_i) dt = I_{LP2} - \frac{V_i}{L_2} t \quad (2)$$

The time interval of first operating mode (τ_1) can be obtained as follows:

$$\tau_1 = \frac{L_e (I_{LP1} + I_{LP2})}{V_i} \quad (3)$$

where L_e is calculated from $[(1/L_1) + (1/L_2)]$.

Second operating mode: At τ_1 , first operating mode ends and second operating mode starts. Owing to the fact that the sum of inductors current is negative, thus, D_1 is off and S_1 is on. At the start of the second operating mode, voltage and current of S_1 is zero, thus, this switch turns on with ZVS and zero current switching (ZCS). The ZVZCS causes decrease in power losses.

The time interval of first and second operating modes is DT_s , in which one of elements S_1 or D_1 is on. Zero crossing time of current through L_1 in time interval DT_s occurs at t_1 . The maximum voltage across C_1 occurs in time interval DT_s at t_2 . In this moment, the current through it is equal to zero. t_1 and t_2 are calculated from (1) and (2) as follows:

$$t_1 = \frac{L_1}{V_i} I_{LP1}, \quad t_2 = \frac{L_2}{V_i} I_{LP2} \quad (4)$$

The maximum value of voltage across C_2 at t_p . In this moment, current through it is equal to zero. t_2 is obtained as follows:

$$t_p = \frac{L_2 (I_{LP2} - I_o)}{V_i} = \frac{DT_s}{2} \quad (5)$$

The value of I_{LP2} can be calculated as follows:

$$I_{LP2} = I_o + \frac{DV_i}{2L_2 f_s} \quad (6)$$

Third operating mode: In the steady-state, S_1 and S_2 , and D_1 are off, thus the sum of L_1 and L_2 current is negative and flows through D_2 . In this operating mode, the voltage across L_1 is positive and constant, therefore, current through L_1 increases linearly and also energy of that increases. The currents through L_1 and L_2 are calculated as follows:

$$i_{L1} = -i_{C1} = I_{LP1} - \frac{V_i DT_s}{L_1} + \frac{V_{C1}}{L_1} (t - DT_s) \quad (7)$$

$$i_{L2} = I_{LP2} - \frac{V_i}{L_2} DT_s + \frac{V_{C1}}{L_2} (t - DT_s) \quad (8)$$

The ending moment of the third operating mode (τ_2) can be calculated as follows:

$$\tau_2 = \left(1 + \frac{V_i}{V_{C1}}\right) DT_s - \frac{L_e (I_{LP1} + I_{LP2})}{V_{C1}} \quad (9)$$

Fourth operating mode: At τ_2 , the third operating mode ends and fourth operating mode starts. Due to this fact that the sum of inductors current is positive, thus, D_2 is off and S_2 is on. At the start of the second operating mode, the voltage and current of S_2 is zero, thus, this switch turns on with ZVZCS, which causes a decrease in power losses.

The time interval of the third and fourth operating modes is $(1-D)T_s = D'T_s$, in which one of elements D_2 or S_2 is on. Zero crossing time of current through L_1 in time interval $D'T_s$ occurs at t'_1 , which is calculated from (8) as follows:

$$t'_1 = \frac{(V_i + V_{C1}) DT_s - L_2 I_{LP2}}{V_{C1}} \quad (10)$$

The maximum value of voltage across C_1 occurs in time interval $D'T_s$ at t'_2 . In this moment, current through it is equal to zero. t'_2 is calculated from (7) as follows:

$$t'_2 = \frac{(V_i + V_{C1}) DT_s - L_1 I_{LP1}}{V_{C1}} \quad (11)$$

The minimum value of voltage across C_2 occurs at t_v . In this moment, the current through it is equal to zero. t_v is calculated as follows:

$$t_v = \frac{L_2 (I_o - I_{LP2}) + (V_i + V_{C1}) DT_s}{V_{C1}} = \frac{D+1}{2} T_s \quad (12)$$

Owing to the fact that in the steady-state, average current through capacitors in a switching period is zero [13], thus by using (6) we have:

$$I_{LP1} = \frac{D}{1-D} I_o + \frac{DV_i}{2L_1 f_s} \quad (13)$$

Currents through L_1 and L_2 in terms of the output current are obtained respectively as follows:

$$I_{L1} = \frac{D}{1-D} I_o \quad (14)$$

$$I_{L2} = I_o \quad (15)$$

Fig. 2 shows key waveforms of the BQ-Cuk converter. In this figure, G_{S1} and G_{S2} are triggered pulses of S_1 and, respectively.

The equations of V_{C1} and voltage conversion ratio (M_V) are obtained respectively as follows:

$$V_{C1} = \frac{D}{1-D} V_i \quad (16)$$

Fig. 2. Key waveforms of the BQ-Cuk converter in SD

Fig. 3. Comparison of the BQ-Cuk converter with conventional B-Cuk converter; (a) in terms of voltage conversion ratio; (b) in terms of voltage stress on capacitor

$$M_V = \frac{V_o}{V_i} = \frac{1-2D}{1-D} \quad (17)$$

Fig. 3(a) shows per-unit voltage stress on C_1 in the BQ-Cuk converter and its comparison with the conventional B-Cuk converter. According to this figure, the voltage stress on C_1 in the BQ-Cuk converter is lower than the conventional converter. Fig. 3(b) shows the voltage transfer function of the BQ-Cuk converter and its comparison with B-Cuk conventional converter. According to this figure, the BQ-Cuk converter in addition to providing the voltage transfer ratio of conventional converter can also provide a different transfer ratio.

3. Analysis of Critical Inductances and Different Operating Modes

If the number of operating modes decreases from four to two, in a way that in a switching period only S_1 and D_2 are on, in this case the operation of the BQ-Cuk converter is called S1D2 operation. Also, if the number of operating modes decreases from four to two in a way that in a switching period only S_2 and D_1 are on, in this case the operation of the BQ-Cuk converter is called S2D1 operation.

According to the Fig. 2, the boundary conditions for changing from SD operation to S1D2 operation are as follows:

$$\tau_1 = 0, \quad \tau_2 = T_s \quad (18)$$

Using (3), (9) and considering the condition of (18), critical inductance $L_{e,Crit}^{S1D2}$ is obtained as follows:

$$L_{e,Crit}^{S1D2} = \frac{D(1-D)^2}{-2f_s(1-2D)} R_L, \quad D > 0.5 \quad (19)$$

Also, according to the Fig. 2, the boundary conditions for changing from SD operation to S2D1 operation are as follows:

$$\tau_1 = \tau_2 = DT_s \quad (20)$$

Fig. 4. The boundary areas between various operations for different inductance values, output load and switching frequency in terms of duty cycle; (a) Normalized inductance L_e ; (b) Normalized output load

Using (3) and (9) and considering the condition of (20), critical inductance $L_{e,Crit}^{S2D1}$ is obtained as follows:

$$L_{e,Crit}^{S2D1} = \frac{D(1-D)^2}{2f_s(1-2D)} R_L, \quad D < 0.5 \quad (21)$$

Figs. 4(a) and 4(b) show normalized inductance L_e and normalized output load as a function of the duty cycle.

4. Design Considerations in SD Operation

The design of the proper inductances of inductors is carried out by considering the acceptable range of the current ripple ($x_L\%$). The acceptable range of the current ripple is defined as follows [14]:

$$x_L\% = \frac{I_{LP} - I_{LV}}{I_L} \times 100 \quad (22)$$

By using (22), the rated inductances of L_1 and L_2 in terms of the acceptable range of the current ripple are calculated as follows:

$$L_1 = \frac{R_L(1-D)^2}{(1-2D)f_s x_{L1}\%} \times 100 \quad (23)$$

$$L_2 = \frac{R_L D(1-D)}{(1-2D)f_s x_{L2}\%} \times 100 \quad (24)$$

The proper design of the output capacitor, which is paralleled to the output load, is very important. The acceptable range of the voltage ripple of capacitor ($x_C\%$) is defined as follows [15-17]:

$$x_C\% = \frac{V_{C,max} - V_{C,min}}{V_C} \times 100 \quad (25)$$

By using (25), the capacitance of the output capacitor in terms of $x_{C2}\%$ is calculated as follows:

$$C_2 = \frac{D(1-D)}{8L_2 f_s^2 (1-2D) x_{C2}\%} \times 100 \quad (26)$$

Table 1. The values of selected parameters

Parameters	V_i	R_L	L	C	f_s
Values	60V	55Ω	1.2mH	100μF	10kHz

Fig. 5. Experimental prototype of the BQ-Cuk converter

Fig. 6. Experimental results of the BQ-Cuk converter in SD operation; (a) Current through S_1 with anti-parallel D_1 and voltage across the switch; (b) Current through S_2 with anti-parallel D_2 and voltage across switch; (c) i_{L1} ; (d) i_{L2} ; (e) v_{C1} ; (f) v_{C2}

5. Experimental Results

Fig. 5 shows the experimental prototype of the BQ-Cuk converter. The inductors have a series resistance of 0.2 ohms. The power MOSFETs are IRF840. The value of D is 0.4. The values of other parameters are based on Table 1.

Fig. 6(a) shows the current through S_1 with anti-parallel D_1 . According to this figure, maximum current of D_1 at the start of the first operating mode is almost 2.5A, which coincides with 2.61A obtained from theoretical equations. Also current through S_1 , which is completely corresponded to the theoretical analysis and its maximum

current at the end of the second operating mode is 1.4A. This value almost coincides with 1.39A obtained from theoretical equations. Moreover, Fig. 6(a) shows voltage across S_1 and verifies ZVZCS operation of the BQ-Cuk converter in SD operation. Fig. 6(b) shows the current through S_2 with anti-parallel D_2 which corresponds to the theoretical results. In addition, this figure shows voltage across S_2 and verifies ZVZCS operation of the BQ-Cuk converter in SD operation. Fig. 6(c) shows current through L_1 which its maximum current is almost 1.3A. This value is in agreement with 1.24A calculated from (13). From theoretical equations, the minimum current which flows through it is -0.76A. This value confirms -0.8A obtained from experimental results. Fig. 6(c) also indicates which the average current through L_1 is 0.25A. This value has a little difference with 0.24A calculated from (14). Fig. 6(d) shows current through L_2 which its maximum current is almost 1.4A. This value corresponds to 1.36A calculated from (6). From theoretical equations, the minimum current of L_2 is -0.64A which is confirmed by -0.65A obtained from experimental results. Also, the average current through L_2 is 0.38A, which has a little difference with 0.36A calculated from (15). Fig. 6(e) shows the voltage across C_1 , which completely corresponds to the theoretical analysis carried out in previous sections and confirms the average voltage (40V) from (16). Fig. 6(f) shows the voltage across output capacitor. The average voltage of C_2 calculated from (17) is 20V, which corresponds to the experimental result.

6. Conclusion

In this paper, a ZVZCS topology was proposed for quasi-Cuk converter. Its outstanding advantages are as follows:

- Different voltage and current conversion ratio in comparison with conventional Cuk converter
- Reduced voltage stress on capacitor
- The ability for changing the output polarity
- The capability for increasing or decreasing input voltage
- Bidirectional capability of power flow

The BQ-Cuk converter can operate in SD, S1D2 and S2D1 operations. Analysis of the topology in different operating modes were carried out. In SD operation, the BQ-Cuk converter had four operating modes. By selecting values of different inductances, this converter operates in S1D2 or S2D1 operations. In these operations, the BQ-Cuk converter has only two operating modes. The BQ-Cuk converter can be used as a micro-inverter in various applications. Finally, besides appropriate designing of various elements, experimental results confirmed the accuracy of the ZVZCS topology.

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