Characterization of the Vertical Position of the Trapped Charge in Charge-trap Flash Memory

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Abstract—In this paper, the characterization of the vertical position of trapped charges in the charge-trap flash (CTF) memory is performed in the novel CTF memory cell with gate-all-around structure using technology computer-aided design (TCAD) simulation. In the CTF memories, injected charges are not stored in the conductive polycrystalline silicon layer in the trapping layer such as silicon nitride. Thus, a reliable technique for exactly locating the trapped charges is required for making up an accurate macro-models for CTF memory cells. When a programming operation is performed initially, the injected charges are trapped near the interface between tunneling oxide and trapping nitride layers. However, as the program voltage gets higher and a larger threshold voltage shift is resulted, additional charges are trapped near the blocking oxide interface. Intrinsic properties of nitride including trap density and effective capture cross-sectional area substantially affect the position of charge centroid. By exactly locating the charge centroid from the charge distribution in programmed cells under various operation conditions, the relation between charge centroid and program operation condition is closely investigated.

Index Terms—Charge-trap flash memory, TCAD, macro modeling, silicon nitride, charge centroid, charge distribution

I. INTRODUCTION

Charge-trap flash (CTF) is replacing the floating-gate (FG) flash memory for high-density integration and low-power operation. In the CTF memory cells, the injected charges are not stored in a polycrystalline silicon (poly-Si) conductive layer but in the trapping layer such as silicon nitride ($\text{Si}_3\text{N}_4$). The distribution of trapped charges affects the memory operation of individual cells and needs to be considered in constructing the accurate macro models of CTF memory cells. Although several experiment results have been reported in the previous literature [1-5], the relation between charge distribution and device operation has not been clearly studied yet. In this study, we trace the locations of the trapped charges in the CTF memory cell by device simulations and experimental results in cooperation.

II. SIMULATION AND EXPERIMENTS

For device simulation, a gate-all-around (GAA) channel CTF memory cell is designed by a commercial TCAD tool [6]. In order to consider more realistic circumstances than dealing with a single cell, three memory cells are connected in series between one string select line (SSL) and one ground select line (GSL), which make up a short NAND flash bitline (BL) as shown in Fig. 1(a) and (b). Fig. 1(a) and (b) show the circuit symbol of the simple NAND string with three wordlines (WLs) and the simulated structure,
respectively. In the device simulation, the array structure in Fig. 1(b) is rotated about the axis along the bottom (dotted line in the figure) so that the channel is made to be very thin Si shell on the oxide core. Based on the simulated structure, the GAA-channel CTF memory cells have been fabricated. The oxide-nitride-oxide-nitride-oxide (ONONO) dielectric layers have thicknesses of 2/2/6/6 nm, from bottom to top. The bottom ONO stack is designed for bandgap engineering (BE) to boost the program and erase (P/E) operation speeds [7, 8]. The diameter of the nanowire channel is 40 nm. Ion implantation was not performed for source and drain (S/D) junctions so that the virtual S/D are formed by the gate-to-channel fringing electric field instead [9-11].

III. RESULTS AND DISCUSSION

In order to locate the charge centroid from the relation with charge distribution, the SONONOS CTF memory cells were simulated as shown in Fig. 2(a). Fig. 2(b) shows the transfer curves of the memory cell at the center of the string in Fig. 2(a) before and after the program operation. The charge centroid is calculated from the charge distribution inside the programmed cell by mathematical extraction through Eqs. (1, 2).

\[
Q = \int_0^Tn(x) \, dx
\]

\[
X_{\text{centroid}} = \frac{1}{Q} \int_0^T \frac{Q(x)}{x} \, dx
\]

Here, \(T_n\) is the thickness of nitride trapping layer, \(Q(x)\) is the trapped charge density per unit volume, as a function of vertical distance \(x\). \(Q\) is the density of trapped
charges per unit area throughout the entire Si$_3$N$_4$ layer.

Fig. 3 demonstrates the distributions of the trapped charges inside the nitride trapping layer depending on program time. The program voltage ($V_{\text{PGM}}$) was 16 V and the pulse durations were 10 µs, 100 µs, 1 ms, and 10 ms. As the pulse gets longer, the threshold voltage shift ($\Delta V_T$) becomes larger. The total length of 6 nm in the figure corresponds to the thickness of nitride trapping layer. The left-side boundary is the interface between tunneling oxide and nitride charge trap layer and the right-side one is that between nitride and the blocking oxide.

Fig. 4 depicts the location of charge centroid as a function of $\Delta V_T$ at different $V_{\text{PGM}}$'s. As shown in the figure, the charge centroid migrates from the bottom oxide side to the top oxide side. It is notable that the location of charge centroid depends only on $\Delta V_T$ and is not affected by $V_{\text{PGM}}$. In other words, the same $\Delta V_T$ obtained from different program voltages leads to the same location, which agrees with the previous results [12-14]. However, $x_{\text{centroid}}$ is substantially affected by the intrinsic properties of the trapping nitride layer. When the capture cross-sectional area is large, the injected charges are trapped near the tunnel oxide, which means that the effective capacitance becomes small. On the other hand, in case of small capture cross-sectional area, the programmed charges are located near the blocking oxide, farther from the channel, since the trapping probability gets smaller. The dependence of distribution of trapped charges on capture cross-sectional area is shown in Fig. 5(a). From the $x_{\text{centroid}}$'s extracted from the distributions in Fig. 5(a) by Eqs. (1, 2) are depicted in Fig. 5(b).

Fig. 6 depicts the charge centroid as a function of $\Delta V_T$. As the trap density is low (black square line), the programmed charges are distributed relatively farther from the tunneling oxide interface. On the other hand, in case of high trap density, the distribution is pulled toward the tunneling oxide interface. It should be more probable for the electrons to be trapped near the tunneling oxide interface before travelling across the nitride layer and reaching the nitride/blocking oxide interface as the trap density becomes higher.

In case of low trap density, the trap sites near the tunneling oxide/nitride interface are more readily occupied by the program electrons, and additional charges are not likely to have a high probability to occupy the energy states of the nitride traps. Instead, the surplus program electrons are drifted to the deeper nitride region. Consequently, $x_{\text{centroid}}$ shows an abrupt shift. Fig. 7 shows this process schematically where $J_{\text{trap}}$ is trapping.
current density, $J_{em}$ is emission current density, $J_i$ is electron current density incoming to the $i$th nitride unit volume, and $J_{i+1}$ is electron current density outgoing from the nitride unit volume. In short, under low-trap-density condition, $J_{i+1}$ becomes larger compared with the case of high-trap-density condition and the distribution of trapped electrons becomes wider and changes faster.

V. CONCLUSIONS

In this work, we closely investigated the relation among charge distribution, charge centroid, and program operation conditions. On the initial stage of the program, charge centroid is located between tunneling oxide and the center of nitride charge trap layer. The charge centroid moves toward the blocking oxide since a considerable number of additional program charges are trapped farther from the tunneling ONO-nitride interface as the program voltage gets higher. Also, it has been confirmed that charge centroid has higher dependence on program voltage than program time. Thus, longer charge centroid shift comes with the larger threshold voltage shift resulted from higher program voltage rather than longer program time. Further, it has been proven that effective capture cross-sectional area and trap density play an important role in determining the charge centroid. Both properties can be controlled by process conditions even though the base materials are the same. Capture cross-sectional area and trap density act in the same manner that higher values are more effective in distributing the trapped charges closer to the tunneling oxide/nitride interface. The accurate charge centroid model will make a better way to design processing conditions and operating schemes for precise allocation of the threshold voltages for multi-level/triple-level/X-level cell operations.

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REFERENCES


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