A Novel Zero-Voltage-Switching Push-Pull Forward Converter with a Parallel Resonant Network

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Abstract

A novel zero-voltage-switching (ZVS) push-pull forward converter with a parallel resonant network is presented in this paper. The novel topology can provide a releasing loop for the energy storage in a leakage inductor for the duration of the power switching by the resonant capacitors paralleled with the primary windings of the transformer. Then the transformer leakage inductor is utilized to be resonant with the parallel capacitor, and the ZVS operation is achieved. This converter exhibits many advantages such as lower duty-cycle losses, limited peak voltage across the rectifier diodes and a higher efficiency. Furthermore, the operating principles and key problems of the converter design are analyzed in detail, and the ZVS conditions are derived. A 500W experimental converter prototype has been built to verify the effectiveness of the proposed converter, and its maximum efficiency reaches 94.8%.

Key words: High efficiency, Parallel resonant, Push-pull forward, Zero voltage switching (ZVS)

I. INTRODUCTION

In applications where the input source exhibits a low voltage and a high current, such as photovoltaic energy and fuel cells, the push-pull converter is a desirable DC-DC converter topology. Compared with the conventional push-pull converter, the push-pull forward converter (PPFC) can solve the problems of high turn-off voltage spikes across switches and it can improve the efficiency of the magnetic core [1]. In order to further improve the efficiency and reduce the size, the technology of integrated magnetics is applied [2], [3]. All of the magnetic components including the input filter inductor, step-down transformer and output filter inductors are integrated into a single EE core. Moreover, the improved structure can make the converter more compact and less expensive. A novel PPFC has been proposed to achieve a high reliability and high input voltage applications in [4]. In this topology, the high utilization factor of the transformer is achieved by using two forward cells coupled via an integrated magnetizing core and operating the two cells in an interleaving fashion. In addition, the high reliability is guaranteed since no direct-short path exists in the proposed converter.

A three-level converter has been proposed to reduce the voltage stresses of the switches, the size of the input filter and the output filter [5]. A novel three-level PPFC has been proposed to reduce both the input current ripple and the output filter inductor current ripple in [6], [7]. Moreover, the voltage stress of the rectifier diode can be reduced by this control strategy and an appropriate external paralleled capacitor. However, in three-level topologies, the circuit topology needs more active devices and the drive circuit is complicated.

In order to increase the power density and to reduce the size and weight of the magnetic element, the switching frequency needs to be increased. Then, the turn-off voltage spikes of the transistors cannot be eliminated in the hard switching mode for the conventional PPFC, resulting in severe EMI and a high switching loss. In the dc-dc converter family, soft-switching technology is proposed to solve the above mentioned problems [8], [9]. An LCL resonant Push-Pull dc/dc converter was presented in [10], [11], with C-L resonant components located behind the output stage rectifiers. The MOSFET switches in the primary side operate under the zero-voltage switching (ZVS) conditions due to the
commutation of the transformer magnetizing current and the snubbing effect of the inherent drain-source capacitance. A pair of auxiliary circuits was added to the primary side of the transformer to clamp the voltage spike and to recycle the energy trapped in the leakage inductors in [12]. As a result, the main switches can be turned on with ZVS.

In isolated bidirectional applications, the symmetric structure with the phase-shift control enables the ZVS operation for all of the power switches in [13]. The low voltage side used a push-pull structure and the high voltage side employed a full bridge structure in [14-15]. With the phase-shift control strategy, all of the switches operate under the ZVS condition.

However, only a few articles demonstrate that PPFCs can operate under the ZVS condition. A push-pull forward half-bridge bidirectional dc-dc converter was presented in [16], with all of the switches operating under zero-voltage using the phase-shift control strategy. However, the half-bridge part works in the boost mode when the voltage is step-up, resulting in adverse effects on the dynamic characteristics. At the same time, the effective duty ratio is lost and the conversion efficiency decreases. The magnetizing current was used to achieve the ZVS operation for the switches in the improved PPFC in [17]. The magnetizing inductance should be sufficiently small. Therefore, the transformer must be designed with the appropriate air-gap. However, a small magnetizing inductance causes a large magnetizing current. As a result, all the no-load loss, the reactive current and current stress increases.

As shown in Fig.1, a novel zero voltage switching push-pull forward converter with a parallel resonant network is proposed. The converter is analyzed and designed. Due to the presence of parallel capacitors and transformer leakage inductors, the resonance makes the switches maintain zero voltage switching even under light loads. The proposed converter operates with soft-switching, which reduces the switches losses and rectifier diodes turn-off voltage. The efficiency can be significantly enhanced.

This paper is organized as follows. The steady-state operation and different intervals of operation in the proposed converter are analyzed in Section II. The design issue of the converter is described in detail in section III. Simulation results using SABER are demonstrated to verify the analysis and design in IV. A 500W laboratory prototype has been built and tested to validate the operation of the proposed converter in the analysis of the ZVS. Section IV presents some experimental results, and Section V provides some conclusions.

II. OPERATION AND ANALYSIS OF THE CONVERTER

Fig. 1 shows the main circuit of the proposed converter. It is a novel zero voltage switching push-pull forward converter with a parallel resonant network. In this figure, $U_{in}$ is the input voltage, $Q_1$ and $Q_2$ are the main power switches, and $D_1$ and $D_2$ are the anti-parallel body diodes corresponding to $Q_1$ and $Q_2$ respectively. $C$ is the clamping capacitor, $L_{\text{leak1}}$ and $L_{\text{leak2}}$ are the leakage inductances of the windings $T_{p1}$ and $T_{p2}$, $L_{m1}$ and $L_{m2}$ are the magnetizing inductances of the windings $T_{p1}$ and $T_{p2}$, $C_{l1}$ and $C_{l2}$ are the parallel resonant capacitors, $D_{1}-D_{4}$ are the rectifying diodes, and $L_{f}$ and $C_{f}$ are the output filter inductor and capacitor, respectively. The turn ratio of the transformer is $n=1:1:N$. The proposed converter works in the PWM mode. The duty cycle of the gating signal for the switches $Q_1$ and $Q_2$ is approximately 0.5, and their phase shift is $180^\circ$. There are 10 intervals in one cycle. The main waveforms are shown in Fig. 2.

The following assumptions are made before analyzing the converter operation principles:

a) All of the semiconductor devices are ideal and lossless.

b) All of the inductors, capacitors and transformer are ideal.

c) $C_{l1}$ and $C_{l2}$ are equal i.e., $C_{l1}=C_{l2}=C_{l}$.

d) The leakage inductances of the transformers are equal i.e., $L_{\text{leak1}}=L_{\text{leak2}}=L_{\text{leak}}$ and the magnetizing inductance is large enough.

e) The two parallel resonant capacitors are equal i.e., $C_{l1}=C_{l2}=C_{l}$.

The operation principle is only analyzed in the first half cycle. In the second half cycle, these intervals are the same as...
those in the first half cycle, and the other symmetrical devices conduct. Fig. 3 illustrates the equivalent circuits in different modes of operation for the first half cycle.

A. Interval 0 (Fig. 3(a): t0<t<t1)

In this interval, the transistor Q2 and the diodes D2 and D3 are conducting. The voltage source energy is transferred to the load by loop1, $U_{in}-L_{leak2}-T_{es}-Q_{2}-U_{in}$, and loop2, $C-Q_{2}-L_{leak1}-T_{pl}-C$. At the end of this interval, the current $i_1$ reaches its minimum value and the current $i_2$, which flows through the magnetizing inductors, increases to its maximum value.

B. Interval 1 (Fig. 3(b): t1<t<t2)

At $t=t_1$, the transistor Q2 is turn off. Q2 can achieve zero-voltage turn-off if the capacitors $C_{t2}$ and $C_{L2}$ are large enough.

During this interval, the rectifier diodes $D_2$ and $D_3$ are conducting while $D_1$ and $D_4$ are turned OFF. The output filter inductor $L_f$ is transformed to the primary side to resonate with the leakage inductors of the transformer, $C_{t2}$, $C_{L2}$, $C_{v1}$ and $C_{L1}$. Consequently, the capacitors $C$ and $C_{v2}$ are charged and the capacitor $C_{t2}$ gets to be discharged by the current $i_2$. The voltage $u_{c2}$ (i.e., $u_{d2}$) rises up from zero while $u_{c1}$ falls down from $U_{in}$. Meanwhile, the capacitors $C_{t1}$ and $C_{v1}$ are discharged by $i_1$. As a result, the voltage $u_{c1}$ (i.e., $u_{d1}$) starts falling down from $2U_{in}$ and $u_{c1}$ also begins falling down from $U_{in}$. In this mode, $i_2$ decreases slowly and $i_1$ decreases reversely. Accordingly, $i_{d2}$ also decreases. At the end of this interval, the current $i_1$ decreases to zero. The node voltage equations are established as shown in Equ. (1).

$$
i_1 = \frac{[i_1(t_1) + i_1(t_2)]}{2} \cos(\omega(t - t_1)) + \frac{I_p}{2}$$

$$i_2 = \frac{[C_1 + C_2][i_2(t_2) + i_2(t_1)]}{2[2(C + C_1 + C_2)]} \cos(\omega(t - t_1)) - \frac{I_p}{2}$$

$$u_p = U_{in} + \frac{I_p}{2(C_1 + C_2)}(t - t_1) + \frac{L_{leak}I_p\delta(t - t_1) - L_{leak}i_1(t_1)\delta(t - t_1)}{2}$$

$$u_{d1} = 2U_{in} + \frac{I_p}{2(C_1 + C_2)}(t - t_1) - \frac{L_{leak}[i_1(t_1) + i_2(t_1)]}{2\omega}\sin(\omega(t - t_1))$$

$$u_{d2} = \frac{L_{leak}[i_1(t_1) + i_2(t_1)]}{2\omega}\sin(\omega(t - t_1)) - \frac{I_p}{2(C_1 + C_2)}(t - t_1)$$  

where:

$$\omega = \frac{1}{\sqrt{2CL_{leak} + C_1L_{leak} + C_2L_{leak}}}, I_p = i_1 - i_2 < 0,$$

At $t=t_2$:

$$i_1 = 0$$

$$i_2 = -I_p$$

$$u_{d1} = u_{d2} = 0$$

By solving Eqns. (1) and (2), the duration can be derived by:

$$t_{d2} = \frac{-2U_{in}(C_1 + C_2)}{I_p}$$  

C. Interval 2 (Fig. 3(c): t2<t<t3)

At $t=t_2$, the current $i_1$ decreases to zero reversely, and starts increasing. The capacitor $C_{t1}$ can be charged by $i_1$. Meanwhile, the current $i_2$ continues decreasing and the capacitors $C_{t2}$ and $C_{L2}$ are charged. In this interval, the values of $i_1$ and $i_2$ are positive so that the rectifier diodes $D_1$-$D_4$ are conducting. Correspondingly, the current $i_{d1}$ increases and $i_{d2}$ decreases.

The second winding is in the freewheeling state. In this mode, the leakage inductor of the transformer $L_{leak2}$ is resonant with the parallel resonant capacitors $C_{t2}$ and the junction capacitors $C_{L2}$. At $t=t_3$, the voltage $u_{c2}$ increases to $2U_{in}$ and $u_{c1}$ reaches zero. The anti-parallel body diodes of the transistor $Q_2$ can be naturally conducted. According to the calculation method in interval 1, the equations for this interval are shown as:

$$i_1 = \frac{\omega C(U_{in} - U_{d2})\sin(\omega(t - t_2)) - \frac{I_p}{2}\cos(\omega(t - t_2))}{2} + \frac{I_p}{2}\cos(\omega(t - t_2))$$  

$$i_2 = \frac{\omega C(U_{in} - U_{d2})\sin(\omega(t - t_2)) - \frac{I_p}{2}\cos(\omega(t - t_2))}{2} + \frac{I_p}{2}\cos(\omega(t - t_2))$$  

$$u_{d2} = \frac{L_{leak}[i_1(t_1) + i_2(t_1)]}{2\omega}\sin(\omega(t - t_1)) - \frac{I_p}{2(C_1 + C_2)}(t - t_1)$$
During this interval, the value of \( i_2 \) dropped to zero before conducting \( Q_1 \). The clamp capacitor \( C \) acts on the leakage inductor of the primary winding \( T_{p2} \). The voltage on the leakage inductor of the winding \( T_{p1} \) is the voltage source \( U_{in} \). The current \( i_2 \) is decreasing while \( i_1 \) is rapidly increasing. During this interval, the value of \( i_2 \) is still higher than \( i_1 \). This interval ends when the transistor \( Q_1 \) conducts.

\[ i_2 = \frac{-l_2}{2} \cos[\omega(t-t_2)]-\frac{l_2}{2} \cos[\omega(t-t_3)] \]

\[ u_{d1} = U_{in} \frac{-\alpha L_{in} I_{p2}}{2} \sin[\omega(t-t_2)] \]  \hspace{1cm} (4b)

\[ u_{d2} = U_{in} \frac{-\alpha L_{in} I_{p2}}{2} \sin[\omega(t-t_3)] \]  \hspace{1cm} (4c)

At the end of this mode, the voltage \( u_{d1} \) reaches zero. As a result, the transistor \( Q_1 \) can achieve zero voltage turn on. Therefore, the duration of this interval is shown as:

\[ t_{23} = \frac{[U_{in}(C + C_j + C_p) + CU_j(C_i + C_j)]}{CI_p} \]  \hspace{1cm} (5)

where:

\[ U_c = U_{in} + \alpha L_{in} [i_1(t_{11}) + i_2(t_{12})] \sin[\frac{2\alpha U_{in}(C_i + C_j)}{I_p}] \]  \hspace{1cm} (6)

\[ D. \text{ Interval } 3 \text{ (Fig. 3(d))}: t_3 < t < t_4 \]

At \( t=t_3 \), the anti-parallel body diode of the transistor \( Q_{p1} \) is turned on. The clamp capacitor \( C \) acts on the leakage inductor of the primary winding \( T_{p2} \). The voltage on the leakage inductor of the winding \( T_{p1} \) is the voltage source \( U_{in} \). The current \( i_2 \) is decreasing while \( i_1 \) is rapidly increasing. This interval ends when the transistor \( Q_1 \) conducts.

\[ E. \text{ Interval } 4 \text{ (Fig. 3(e))}: t_4 < t < t_5 \]

At \( t=t_4 \), the transistor \( Q_1 \) is conducting. The voltage \( u_{d1} \) has dropped to zero before conducting \( Q_1 \). The procedure for the operation in this interval is similar to that in the last interval. The currents \( i_1 \) and \( i_2 \) through the transformer during this interval are determined as follows:

\[ \begin{align*}
  i_1 &= i_1(t_{11}) + \frac{U_{in}}{L_{in}}(t-t_4) \\
  i_2 &= i_2(t_{12}) + \frac{U_{in}}{L_{in}}(t-t_4)
\end{align*} \]  \hspace{1cm} (7)
During this interval, the current increases from \( I_{i, \text{min}} \) to \( I_{i} \). Therefore, the duration of this interval is shown as:

\[
\tau_d = \frac{nI_{\text{link}}I_{i, \text{min}}}{U_{in}[1+i_1(t_{i1})/i_1(t_{i})]}
\]  

(8)

F. Interval 5 (Fig. 3(f): \( t_5 < t < t_6 \))

The current \( i_2 \) reached zero at the end of the last interval. In this interval, the voltage across the winding \( T_{p2} \) is the clamp inductor \( L_{\text{Leak}} \) and the above intervals repeat in the same sequence with the other symmetrical devices conducting in the second half cycle.

III. CONVERTER DESIGN

A. Voltage and Current Stress of the Semiconductor Devices

The maximum voltage across the main power transistors \( Q_1 \) and \( Q_2 \), is \( 2U_{in} \). The rms current through the primary switches is shown as:

\[
i_{Q1} = i_{Q2} = n P_0 / \eta U_0
\]

(10)

where \( n \) is the turns ratio of the transformer, \( P_0 \) is the output power, \( U_0 \) is the output voltage, and \( \eta \) is the conversion efficiency.

The RMS current through the rectifier diodes \( D_1-D_4 \) is given as:

\[
i_{D1} = i_{D2} = i_{D3} = i_{D4} = P_0 / 2\eta U_0
\]

(11)

B. ZVS Realization Condition

Based on the above mentioned analysis, it can be concluded that when this circuit works in the stage of interval 1, the equivalent inductors of the primary windings, which originate from the transformation of \( L_{\text{link}} \) and \( L_{l} \), resonate with the parallel capacitor and parasitic capacitor. The energy saving in \( L_{l} \) is adequate to make the discharge voltage of \( C_{v2} \) decrease to zero, and is easy to achieve ZVS. However, when the circuit works in interval 2, only \( L_{\text{link}} \), the parallel capacitor and the parasitic capacitor resonate. Due to the fact that \( L_{\text{link}} \) is far less than \( L_{s} \), it is more difficult to achieve zero-voltage turn-on than zero-voltage turn-off for \( Q_1 \). As long as the novel topology meets the zero-voltage turn-on conditions, the ZVS for \( Q_1 \) and \( Q_2 \) can be accomplished.

Taking \( Q_1 \) as an example, it is necessary to ensure that \( u_{ds1}=0 \) before turning on the transistor \( Q_1 \) to achieve the zero-voltage turn-on for \( Q_1 \). According to interval 3, formula (5) can be used to calculate the time at which the voltage across \( C_{v1} \) decreases to zero from \( U_{in} \). Thus, the dead-time is derived as:

\[
t_d > t_{12} + t_{35} = \frac{2U_{in}(C_{v1} + C_{v2})}{I_p} \left[ U_{in}(C_{v1} + C_{v2}) + C_{v2}U_{in} \right] \]

(12)

where \( t_d \) is the dead-time.

In addition, the capacitor \( C_{v1}, C_{v2} \) and \( C_{v3} \) are charged by the energy saved in \( L_{\text{link}} \). The energy has to be adequate to make the voltage \( u_{C_{v3}} \) increase to \( U_{in} \) from 0, to make \( u_{C_{v3}} \) decrease to \( U_{in} \) from 0, and to make \( u_{C_{v2}} \) increase to \( 2U_{in} \) from \( 0 \). Thus, the energy condition to achieve ZVS is determined by:

\[
E_{\text{link}} \geq E_{C_{v1}} + E_{C_{v2}} + E_{C_{v3}}
\]

(13)

Ignoring the current ripple, formula (13) can be derived as:

\[
L_{\text{link}} \left( \frac{P_0}{2\eta U_0 D} \right)^2 > C_{v1}U_{in}^2 + \frac{3C_{v1}}{2}U_{in}^2 \Rightarrow
\]

(14)

Formulas (12) and (14) indicate that heavy loads and high leakage inductances are conducive to achieving ZVS.

C. Duty Cycle Loss

During interval 3, although the voltage across the primary transformer winding is positive, the current is too low to provide energy to the load. All of the rectifier diodes are conducting. As a result, the voltage across the secondary winding is zero, which produces duty cycle losses. During interval 1, the primary side is in the stage of dead-time. Meanwhile, due to parallel resonant capacitance, the currents \( i_1 \) and \( i_2 \) slowly decrease. Therefore, the voltage across the secondary winding is negative in mode1. Thus, the duty cycle loss in the novel ZVS PPF can be lower than that in the conventional PPF. The duty cycle loss can be shown as:

\[
D_{\text{loss}} = \frac{2nI_{\text{link}}I_{i, \text{min}}}{U_{in}T_s[1+i_1(t_{i1})/i_1(t_{i})]} + \frac{4U_{in}(C_{v1} + C_{v2})}{T_sI_p}
\]

(16)

where \( T_s \) is switching period.

Formulas (16), increases in the transformer leakage inductance increase the amount of \( D_{\text{loss}} \) in the converter. Thus, the parallel resonant capacitance \( C_{l} \) cannot be designed so large that it is not conducive to the ZVS of the transistors. Therefore, an appropriate \( L_{\text{link}} \) needs to be appreciated.

D. Parameters of the Resonant Network

According to the ZVS realization condition, \( L_{\text{link}} \) and \( C_{l} \) can be calculated when the main circuit parameters are determined.
1) **Parallel Resonant Capacitor C**: Assuming that the clamp capacitor C is large enough, the voltage across C \((U_c)\) is constant \((U_c=U_{in})\). According to equation (12), the dead time \(t_d\) can be obtained by:

\[
t_{d_{\text{min}}} \geq \frac{4U_{in}(C_1 + C_L)}{I_p} - \frac{U_{in}(C_1 + C_L)^2}{2U_{in}}
\]

where \(t_{d_{\text{min}}}=10\%T_s\). \(T_s\) is the switching period. The parallel resonant \(C_1\) can be calculated from (17) by:

\[
C_{1_{\text{max}}} = \frac{C_1\sqrt{4U_{in}^2 - 4U_{in}I_{d_{\text{min}}}I_p/C}}{2U_{in}} - 2C
\]

2) **Leakage Inductance \(L_{\text{leak}}\)**: According to \(C_L\) and equation (14), the leakage inductance \(L_{\text{leak}}\) can be expressed as:

\[
L_{\text{leak}} \geq \frac{(4C_L + 9C_i/2)U_{in}\mu^2D^2}{P_0^2}
\]

As long as \(L_{\text{leak}}\) meets equation (19), where \(C_L\) reaches its maximum, the minimum of \(L_{\text{leak}}\) is given as:

\[
L_{\text{leak}_{\text{min}}} = \frac{(4C_L + 9C_i/2)U_{in}\mu^2D^2}{P_0^2}
\]

IV. **The Simulation and Experimental Results**

The conventional push-pull forward topology and the proposed push-pull forward topology have been simulated in Saber. The main specifications are \(U_{in}=10\)V to 14V, \(U_{o}=90\)V, \(P_0=500\)W and \(f=50\)KHz, with a load light output 20\% of \(P_0\) (100W). The main circuit parameters are \(C=10\)μF, the output filter capacitor \(C_f=470\)μF, the output filter inductor \(L_f=200\)μH, the dead time \(t_{d_{\text{min}}}=10\%T_s\), \(C_{1_{\text{max}}}=2\)μF (according to formula (18)), and \(L_{\text{leak}_{\text{min}}}=0.26\)μH (according to formula (19)).

Simulation results are shown in Fig. 4 (a) and (b). In Fig. 5 (a), when \(C_L=0.1\)μF, the novel ZVS PPFC cannot achieve ZVS. This is because \(C_L\) is too small to satisfy formula (12). When \(C_L=0.5\)μF < \(C_{1_{\text{max}}},\) the voltage across \(C_1\) reaches \(U_{in}\) before turning on \(Q_1\). Thus, \(u_{ds1}\) can be clamped to zero, and it can achieve ZVS as shown in Fig. 5 (b). The simulation results show good agreement with the theoretical analysis.

Simulation results with various leakage inductances are shown in Fig. 5(c) and (d). The greater the leakage inductance \(L_{\text{leak}}\), the more easily the ZVS can be achieved. However, when \(L_{\text{leak}}=0.1\)μH (\(L_{\text{leak}_{\text{min}}}>\) ), the zero voltage turning-on cannot be achieved. This is consistent with formula (14). Furthermore, simulation results under the load condition are given in Fig. 5(e). \(u_{ds1}\) decreases to zero at the moment of turning on \(Q_1\). This is consistent with formula (15). Greater values of \(P_0\) and \(L_{\text{leak}}\) result in more energy being stored in the transformer leakage inductor. Energy charges the parallel resonate capacitor \(C_1\) until the voltage across \(C_1\) reaches \(U_{in}\). As a result, the voltage \(u_{ds1}\) is clamped to zero. Therefore, under the load condition, the effect of ZVS is non-ideal compared with the full load condition.

The principal parameters and components are listed in Table I. A 500W experimental converter prototype has been built based on the above theoretical analysis and preliminary simulations, as shown in Fig. 6.

Experimental tests are performed prior to comparing the measured waveforms of the conventional push-pull forward converter and the novel push-pull forward converter under various load conditions to evaluate the advantages and disadvantages of the novel ZVS PPFC. The conventional push-pull forward converter experimental waveforms are shown in Fig. 7(a). It can be seen that the turn-off voltage...
Fig. 5. $u_{gs1}, u_{ds1}, i_{ds1}$ waveforms under different parameters conditions for the proposed novel ZVS PPFC.

(a) $C_L=0.1\mu F$ at $P_0=500W$.

(b) $C_L=0.5\mu F$ at $P_0=500W$.

(c) $L_{\text{Leak}}=0.1\mu H$ at $P_0=500W$.

(d) $L_{\text{Leak}}=0.2\mu H$ at $P_0=500W$.

(e) $C_L=0.5\mu F$, $L_{\text{Leak}}=0.1\mu H$ at $P_0=100W$.

Fig. 5. $u_{gs1}, u_{ds1}, i_{ds1}$ waveforms under different parameters conditions for the proposed novel ZVS PPFC.

TABLE I

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Mosfets $Q_1, Q_2$</td>
<td>IRFB3607Pbf</td>
</tr>
<tr>
<td>Clamp capacitor C</td>
<td>$10\mu F$, $100V$ CBB capacitor,4 capacitors in parallels</td>
</tr>
<tr>
<td>Parallel resonate capacitor $C_{L1}, C_{L2}$</td>
<td>$0.47\mu F$ and $0.1\mu F$ CBB capacitors in parallel</td>
</tr>
<tr>
<td>EE4220/818/H ferrite core, Primary windings</td>
<td>turns: $n_1=n_2=2$; secondary turns $n_3=23$; Leakage inductance referred to the primary $L_{\text{leak}}=0.4\mu H$</td>
</tr>
<tr>
<td>HF Transformer</td>
<td>MUR1005FCT</td>
</tr>
<tr>
<td>Rectifier diodes</td>
<td>MUR1005FCT</td>
</tr>
<tr>
<td>Output filter inductor $L_f$</td>
<td>$200\mu H$, $10A$</td>
</tr>
<tr>
<td>Output filter inductor $C_f$</td>
<td>Two $470\mu F$,$200V$ electrolytic capacitors and $0.1\mu F$ $250V$ CBB capacitors</td>
</tr>
</tbody>
</table>

Fig. 6. 500W prototype of the proposed novel ZVS PPFC.

spike of $Q_1$ reaches $46V$ under the full load condition, which is more than twice $2U_{in}$. The voltage across the transformer secondary side $u_{AB}$ exhibits high spikes ($320V$), which increase the requirements for the rectifier diodes. The switching loss also increases. Accordingly, high voltage
spikes damage the switching elements easily. The turning-on and turning-off processes for transistor $Q_1$ are shown in Fig. 7(b) and (c). The EMI is severe at the moment of turning on and turning off. Obviously, the turning-off voltage spike of transistor $Q_1$ approaches 46V because of the existence of leakage inductance.

At the moment of turning off ($Q_1$), back electromotive force can be generated across the leakage inductance of the transformer. Therefore, the voltage $u_{ds1}$ is higher than $2U_{in}$. A larger leakage inductance results in a higher turning-off voltage spike. Thus, ZVS for the transistor $Q_1$ cannot be achieved.

Fig. 8(a) presents the novel push-pull forward converter experiment results at $L_{leak}=0.1\mu H$ and $P_0=500W$. It can be seen that the maximum value of the voltage across $u_{ds1}$ is $2U_{in} = 24V$ under the full load condition.

This demonstrates that the novel push-pull forward converter can eliminate the turn-off voltage spikes. Meanwhile, the maximum value of the secondary winding voltage $u_{AB}$ is 250V. The voltage stress of the rectifier diodes
can be reduced. The EMI at the moment of turning-on and turning-off in Fig. 8(b) and (c) are much smaller than those in Fig. 7(b) and (c) due to the introduction of the parallel capacitor $C_L$. Moreover, the voltage $u_{ds1}$ decreases to zero before turning on $Q_1$. Similarly, the voltage $u_{ds1}$ is kept at zero until the turning on of $Q_1$. Thereby, ZVS can be achieved.

The novel push-pull forward converter experiment results under the light load condition are shown in Fig. 9. As shown in Fig. 9(a), the maximum value of the voltage across $u_{ds1}$ is $2U_{in}=24V$. Meanwhile, the maximum value of the transformer secondary voltage $u_{AB}$ is 240V with lower voltage spikes. The duty cycle loss is reduced under the light load condition when compared with the full load condition. This meets formula (16). A smaller value of $I_{L_{min}}$ results in a smaller $D_{loss}$. The processes of turning-on and turning-off are shown in Fig. 9 (b) and (c). It is still possible to achieve ZVS. Obviously, the novel push-pull forward converter can achieve ZVS over a wide load range.
strategy is the same as that in the conventional push-pull forward converter. A 500W experimental converter prototype has been built and the conclusions are drawn as follows:

1) The novel zero voltage switching (ZVS) push-pull forward converter has the advantages of the conventional push-pull forward converter, along with the ability to reduce or even eliminate the cut-off voltage spikes.

2) The proposed converter topology can operate in the ZVS mode over a wide load range. It is conducive to improving the efficiency and increasing the switching frequency.

3) The converter proposed in this paper can reduce the duty cycle loss and improve the voltage gain.

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