A Phase Current Reconstruction Technique Using a Single Current Sensor for Interleaved Three-phase Bidirectional Converters

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Abstract-This paper proposes a new phase current reconstruction technique for interleaved three-phase bidirectional dc-dc converters using a single current sensor. In the proposed current reconstruction algorithm, a single current sensor is employed at the dc-link, and the dc-link current information is sampled at either the peak or valley point of the pulse-width modulation (PWM) carriers regularly. From the obtained current information, all phase currents are reconstructed in a single PWM cycle. After that, the digital current controller is applied to achieve current balancing in each phase. Compare to the previous multiple current sensor method, the proposed strategy reduces the number of the current sensors in the interleaved three-phase bidirectional converter as well as reducing potential current sensing error caused by non-ideal characteristics of the multiple current sensors. The effectiveness of the proposed method is verified from the experiments based on a 3kW three-phase bidirectional converter prototype for the automotive battery charging application.

Keywords: Interleaved converter, Current reconstruction, Single current sensor, Digital control

1. Introduction

Multi-phase interleaved dc-dc converters have been popularly employed in many power conversion applications such as automotive bidirectional battery chargers, renewable energy interface converters, computer power supplies, and so on [1-7]. One of the well-known problems of the multi-phase dc-dc converter is that each phase's current can be different under their operation, and this current imbalance may deteriorate the efficiency and the stability of the multi-phase converter. Hence, the each phase current should be controlled by using an adequate current balancing or sharing strategy.

In order to implement the current sharing feature, many studies have been conducted [3, 8-18]. In [3], the multiple sensors and controllers are employed to control the individual phase current in real-time. Reference [8] proposes the simple RC network circuit to measure the multiple phase currents, and the current sharing control is applied. However, the methods mentioned above essentially require multiple current sensors which increase the implementation cost and the measurement error caused by uneven sensor gains. On the other hand, the current sensorless techniques have been proposed to implement the current sharing performance without any current sensors [10, 11]. Reference [10] implements the current sensorless method to achieve the current sharing as well as the

efficiency improvement. However, this method cannot be directly applicable to current control applications such as battery chargers. In [11], the small signal perturbation technique is implemented to estimate the phase currents without current sensors. However, this method has a problem with low dynamic performance due to delays caused by the perturbation and measurement.

To overcome these limitations of the previous methods, single current sensor techniques have been arisen for the interleaved multiphase dc-dc converter applications where both the voltage and the current control are necessary. In fact, using a single current sensor has been issued in the inverter applications [12-15]. Recently, the single current sensor techniques have been also studied for the multiphase dc-dc converter applications [16-18]. In [16], only one current sensor is employed at the dc-link to measure the phase currents of multiple phases. However, this method requires the additional switch modules to guarantee the current measuring operation. In [17], the dc-link current is measured, and the phase currents are reconstructed for the interleaved two-phase dc-dc converter. However, this method cannot be directly applied for multiple phases where the number of the phases is greater than two. Recently, in [18], a single current sensor strategy where the current reconstruction is guaranteed in a PWM switching cycle is proposed for the interleaved four-phase dc-dc converter.

This paper proposes a single current sensor method for the interleaved three-phase bidirectional dc-dc converter. In this paper, the method proposed in [18] is modified for the three-phase bidirectional dc-dc converter.

The proposed method consists of the current reconstruction and individual phase current control. In the

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proposed current reconstruction algorithm, a single current sensor is placed at the dc-link, and the current sensor output is sampled at either the peak or the valley point of the pulse-width modulation (PWM) carrier regularly. To the obtained current information, the current reconstruction algorithm is applied according to the duty reference of the controller output. By using the reconstructed phase current information, the digital current controller is easily applied to balance the currents in each phase. In addition to this, the modeling and the control of the three-phase dc-dc converter have been carried out. To do this, both the z-domain modeling and the type 3 controller design have been detailed. The effectiveness of the proposed method is verified by the simulations and the experiments based on a 3kW three-phase bidirectional dc-dc converter prototype for the battery charging application.

2. Proposed Current Reconstruction Method

2.1 Fundamental characteristics of the dc-link current

Fig. 1 shows the three-phase interleaved bidirectional dc-dc converter. In the figure, the single current sensor locates between the switching legs and the dc-link capacitor to measure the dc-link current i_{dc} . Table 1 shows the relationship between the switching functions, S_a , S_b , and S_c , and i_{dc} . When a switching function is 1, the upper switch of the corresponding switching leg is turned on. On the other hand, the lower switch is turned-on when the

Fig. 1. Three-phase interleaved bidirectional dc-dc converter with a single current sensor: (a) $S_a=1, S_b=0$ and $S_c=0$; (b) $S_a=0, S_b=1$ and $S_c=1$.

Table 1. The relationship between the switching function and the dc-link current

S_a	S_b	S_c	i_{dc}
0	0	0	0
0	0	1	i_c
0	1	0	i_b
0	1	1	$i_b + i_c$
1	0	0	i_a
1	0	1	$i_a + i_c$
1	1	0	$i_a + i_b$
1	1	1	$i_a + i_b + i_c$

Fig. 2. Waveforms of the phase current and dc-link current. (a) $d < 0.333$, (b) $d > 0.333$

switching function is 0. It should be noticed that the upper and the lower switches are complementary working.

The relationship between the dc-link and the phase currents is simply written as,

$$i_{dc} = S_a i_a + S_b i_b + S_c i_c \quad (1)$$

where i_a, i_b , and i_c represents each phase's current. Eq. (1) shows that the dc-link current can be represented by the combinations of the switching functions and the phase current.

It means that each phase current can be reconstructed from i_{dc} as long as the switching function is known. For example, suppose that $S_a = 1, S_b = 0$ and $S_c = 0$. Then, i_{dc} reflects phase a current i_a . (see Fig. 1(a) and Table 1). For the next, if the switching functions are $S_a = 0, S_b = 1$ and $S_c = 1$, i_{dc} corresponds the sum of phase b and phase c currents as shown in Fig. 1(b) and Table 1.

Fig. 2 illustrates the switching function, the phase current and i_{dc} according to the ranges of the output duty cycle when the system operates as a buck converter. In the case of Fig. 2(a) where the output duty reference d is lower than 0.333, each phase current is shown up at i_{dc} in relays.

For $d > 0.333$, the waveforms are shown in Fig. 2(b). In this mode, any two or three phase current is overlapped periodically. These fundamental characteristics of the dc-link current are employed to reconstruct individual phase

Fig. 3. Relationship among the duty reference, switching function, phase current, dc-link current and sampling point (a) $d < 0.333$, (b) $d > 0.666$, (c) $0.333 < d < 0.666$

currents in this paper.

2.2 Proposed current reconstruction method

The reconstructed current is used instead of actual phase currents to balance the each phase current. For accurate current reconstruction, the following conditions are needed to be satisfied. First, the duty reference should be fixed for a single PWM cycle to reconstruct each phase current in a single switching period. Second, the measuring points of the dc-link current should be fixed to simplify the implementation. By taking these two conditions, the average current of each phase is easily measured.

Fig. 3 represents the relationship among the duty reference, the switching function, the phase current, the dc-link current, and the sampling points in the proposed technique. As shown in the figure, the current sampling point is changed according to the duty reference. As explained in the previous section, when the duty reference is less than 0.333, the dc-link current is sampled at the valley point of each carrier as in Fig. 3(a).

For the other case, under the duty reference higher than 0.666, the dc-link current is measured at the peak of each carrier as shown in Fig. 3(b). For the last case, when the duty reference is between 0.333 and 0.666, the dc-link current is measured at either the valley or the peak of each carrier. This case is shown in Fig. 3(c). Once i_{dc} is measured, it is stored in i_1 , i_2 , and i_3 , at every sampling instant. For current reconstruction, i_1 , i_2 , and i_3 are utilized.

For current reconstruction, first, when the duty reference is less than 0.333, only one phase has the switching function of 1 at the sampling point in Fig. 3(a).

Consequently, the sampled dc-link current becomes naturally the average phase current. Second, when the duty reference is higher than 0.666, two phases have the switching function of 1 at every sampling point. In this case, the sum of two phase currents is occurred at the dc-link. Therefore, the sampled dc-link current is not equal to each phase's average current, and it is represented as follows:

$$\begin{aligned} i_1 &= i_b + i_c \\ i_2 &= i_a + i_c \\ i_3 &= i_a + i_b \end{aligned} \quad (2)$$

where i_1 , i_2 , and i_3 are the dc-link currents measured at the peak points of phase a , b , and c carrier waveforms in the single PWM switching period, respectively.

By manipulating (2), the current relationship can be rewritten as (3):

$$\begin{aligned} i_a &= 0.5 \times (i_3 + i_2 - i_1) \\ i_b &= i_3 - i_a \\ i_c &= i_1 - i_b \end{aligned} \quad (3)$$

Finally, if the duty reference is between 0.333 and 0.666, it is possible to use any of both of the sampling points, the peak and the valley points as shown in Fig. 3(c). If the valley points are selected, only one phase's current is came out at the sampling instant. That is a same situation with the case in Fig. 3(a). Accordingly, the phase current is directly reconstructed by the sampled dc-link current without a calculation. On the other hand, if the dc-link current is sampled at the peak points, two phases have the switching function of 1, and this is also the same situation explained in Fig. 3(b). Hence, Eq. (3) can be employed to reconstruct the three-phase currents.

2.3 Non-reconstruction region analysis for complete reconstruction

In the proposed method, the minimum duty width d_{mw} should be ensured to completely reconstruct the phase current. Here, d_{mw} is the minimum duty interval that is the sum of settling time T_{ir} and analog to digital conversion (ADC) time T_{ad} . If d_{mw} is not large enough to address these issues, and if the duty reference d or $(1-d)$ is less than d_{mw} , the measured dc-link current may not be reliable, and it can be misread as illustrated in Fig. 4(a). These regions are defined as non-reconstruction region, and it can be occurred when duty reference is between 0 and d_{mw} or between $(1-d_{mw})$ and 1. In fact, the converter using the proposed method cannot run in the non-reconstruction region.

To solve this issue, the duty reference is set to be zero by force when its original value is less than d_{mw} . If the original duty reference is more than $(1-d_{mw})$, the duty reference is

Fig. 4. Non-reconstruction region analysis (a) minimum duty width for reconstruction, (b) non-reconstruction region and measuring point according to d

limited to $(1-d_{mw})$. However, these regions are rarely occurred because those regions are not normal operation region in general, and there has been also a dead-time to prevent a shoot-through condition between upper and lower power devices.

In addition to these conditions, the non-reconstruction region may also appear near the zone between d_{mw} and $(1-d_{mw})$ according to the sampling point of the dc-link current. In the region between $(0.333+d_{mw})$ and $(0.666-d_{mw})$, it is possible to reconstruct the each phase current with the dc-link current using the proposed algorithm as in Fig. 4(b).

However, if the duty reference is placed between $(0.333-d_{mw})$ and $(0.333+d_{mw})$, and the dc-link current is measured at the peak point, the current reconstruction is impossible. In this case, it is difficult to obtain the dc-link current value because the transition from one state to another on the switching function of phase a , b and c occur simultaneously. This situation is shown in Fig. 5. Similarly, if the duty reference is positioned between $(0.666-d_{mw})$ and $(0.666+d_{mw})$, and the current sampling point is the valley of the PWM carrier, the current reconstruction is also not possible. These regions should be additionally included in the non-reconstruction region. However, those situations can be easily avoided by changing the sampling point as shown in Fig. 4(b). For example, if the duty reference is $(0.333+d_{mw})$, the non-reconstruction region is eliminated by sampling at the valley point. If duty reference is 0.666, the peak point is used for i_{dc}

Fig. 5. Non-reconstruction region for the measuring point and the duty reference: (a) $d=0.333$ and the peak point sensing; (b) $d=0.666$ and the valley point sensing

Table 2. Current reconstruction under non-reconstruction region

Duty reference	Sampling method
$0 \sim d_{mw}$	Duty reference = 0
$(0.333-d_{mw}) \sim (0.333+d_{mw})$	Valley point sampling
$(0.666-d_{mw}) \sim (0.666+d_{mw})$	Peak point sampling
$1-d_{mw}$	Duty reference = $1-d_{mw}$

sampling. Then, the phase current can be reconstructed without passing the non-reconstruction region. As a result, the proposed reconstruction method is easily adapted in the entire operating range. Table 2 summarizes the current reconstruction methods under non-reconstruction regions.

3. Modeling and Control of the Three-phase DC-DC Converter

3.1 z-domain modeling of the three-phase interleaved dc-dc converter [19, 20]

Fig. 6(a) shows the equivalent circuit of the three-phase interleaved dc-dc converter for the small-signal model equation. The state equation based on the average model of the buck converter is given as (4).

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_C \end{bmatrix} = \begin{bmatrix} \frac{R_o R_c + R_o R_l + R_l R_c}{L_{eq}(R_o + R_c)} & -\frac{R_o}{L_{eq}(R_o + R_c)} \\ \frac{R_o}{C_o(R_o + R_c)} & \frac{1}{C_o(R_o + R_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{D}{L_{eq}} \\ 0 \end{bmatrix} v_{dc_high} \quad (4)$$

$$\begin{bmatrix} i_L \\ v_{dc_low} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{R_o R_c}{R_o + R_c} & \frac{R_o}{R_o + R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix}$$

where v_{dc_high} , v_{dc_low} , i_L , D , C_o , L_{eq} , R_o , R_l , and R_c are the

(a)

(b)

Fig. 6. Equivalent circuit and control structure of the three-phase interleaved dc-dc converter: (a) the equivalent circuit; (b) the control structure

input voltage, the output voltage, the inductor current, the on duty cycle, the filter capacitance, the equivalent inductance, the load resistor, the parasitic resistance of L_{eq} , and the equivalent series resistance of C_o , respectively. By assuming the uniform inductance in each phase, the equivalent inductance L_{eq} can be written as:

$$L_{eq} = L_a \parallel L_b \parallel L_c = \frac{L_a L_b L_c}{L_a L_b + L_b L_c + L_c L_a} \approx 0.333 L_a \quad (5)$$

where L_a , L_b , and L_c are the each phase inductance. From (4), the small signal equation of the system is derived by applying the perturbation signal at the operating point. As a result, the control-to-inductor current transfer function can be written as:

$$G_{id}(s) = \frac{\tilde{i}_L}{\tilde{d}} = \frac{V_{dc_high} (C_o R_o s + C_o R_c s + 1)}{(R_o + R_c) L_{eq} C_o s^2 + [(R_c + R_l) C_o R_o + R_c R_l C_o + L_{eq}] s + R_o + R_l} \quad (6)$$

where $\tilde{d}$ is the perturbed signal of duty cycle, and $\tilde{i}_L$ is the ac signal of the inductor current. It should be noticed that $G_{id}(s)$ only shows the feature of the analog transfer function, and it does not include digital delays such as digital PWM and computation delays. In order to improve the accuracy of the system model, $G_{id}(s)$ should be converted to a z-domain transfer function including the digital delay effects. In this paper, a triangular carrier modulation is implemented, thus the digital PWM delay effect is modeled as (7) [19].

$$G_{pwm}(s) \approx \frac{1}{2} \left(e^{-\frac{(1-D)T_s}{2}s} + e^{-\frac{(1+D)T_s}{2}s} \right) \quad (7)$$

where T_s is the switching period.

Then, $G_{idm}(s)$ which considers the digital PWM delay is given as follows.

$$G_{idm}(s) = G_{id}(s) G_{pwm}(s) \quad (8)$$

After that, $G_{idm}(s)$ is converted into the z-domain. In this process, the computation delay z^{-1} which is induced by the iteration procedure of the control loop in the microcontroller is considered. Finally, the equivalent z-domain transfer function of the converter is obtained as follows.

$$G_{idz}(z) = z^{-1} Z[G_{idm}(s)] \quad (9)$$

By substituting the system parameters in Table 3 into (9),

Table 3. System ratings and parameters

Ratings and parameters	Value
Rated power	3kW
High-side voltage (V_{dc_high})	100V
Low-side voltage (V_{dc_low})	50V
Phase inductance ($L_{a,b,c}$)	2.0mH
Equivalent inductance (L_{eq})	0.666mH
Output capacitance (C_o)	1100μF
Equivalent resistance (R_l)	5mΩ
ESR (R_c)	10mΩ
Switching frequency (f_{sw})	10kHz

Fig. 7. Frequency responses of $G_{idz}(z)$, $G_{cz}(z)$, and $G_{idz}(z)G_{cz}(z)$

the numerical expression of the control-to-inductor current is represented as follows.

$$G_{idz}(z) = \frac{14.96z - 14.43}{z^3 - 1.95z^2 + 0.963z} \quad (10)$$

3.2 Type 3 current controller design

The current control block-diagram is shown in Fig. 6(b). In this paper, the individual phase current controllers with the reconstructed phase currents $\hat{i}_a$, $\hat{i}_b$, and $\hat{i}_c$ are adopted for balancing each phase. The modified type 3 controller design method proposed in [21] is applied for current control.

Generally, the bandwidth (BW) of a digital current controller is selected to be 1/10~1/15 of the switching frequency, and the phase margin (PM) should be secured at least 45 deg. In this paper, the BW and the PM of the controller are selected as 1 kHz and 70 deg, respectively.

Fig. 7 includes the open-loop gain of the control-to-inductor current model obtained by (10). The magnitude and the phase of the open-loop gain are 28.0 dB and 145.7 deg, respectively, which can be confirmed from (10) and Fig. 7. Hence, in order to satisfy the design specification, the gain boost of 0.0398 and the phase boost of 165.7 deg are necessary to make unity gain and phase of 110 deg at the crossover frequency. Consequently, the K-factor is given as (11) using the gain boost and the phase boost, φ_b .

$$K = \left[\tan \left(\frac{PM - (90 - \phi_b) \times \frac{\pi}{180}}{4} + \frac{\pi}{4} \right) \right]^2 \approx 43.98 \quad (11)$$

To improve the accuracy of the digital controller, the frequency pre-warping near the crossover frequency is applied. Then, the new crossover frequency f_{c_wp} which considering the pre-warping and the pole and the zero frequencies f_p and f_z are obtained as (12) and (13):

$$f_{c_wp} = \frac{1}{\pi T_s} \tan(f_c T_s \pi) \quad (12)$$

$$f_p = \sqrt{K} f_{c_wp} \quad f_z = f_{c_wp} / \sqrt{K} \quad (13)$$

where f_c is the crossover frequency. The modified digital type 3 controller is expressed in (14)

$$G_{cz}(z) = \pi f_{c_wp} T_s \frac{G_b}{K} \frac{(z+1)}{(z-1)} \frac{\left(1 + \frac{(z-1)}{\pi f_z T_s (z+1)} \right)^2}{\left(1 + \frac{(z-1)}{\pi f_p T_s (z+1)} \right)^2} \quad (14)$$

where G_b is the gain boost. In result, the controller is designed as follows.

$$G_{cz}(z) = \frac{0.04569z^3 - 0.0319z^2 - 0.04466z + 0.0329}{z^3 - 0.741z^2 - 0.242z - 0.0167} \quad (15)$$

The frequency response of $G_{cz}(z)$ is also shown in Fig. 7. It is confirmed that the z-domain open-loop gain $G_{cz}(z)G_{idz}(z)$ has the crossover frequency of 1kHz, and the PM of 70 degree, which means that the designed digital current controller satisfies the design specification exactly.

3.3 System operation sequences

The microcontroller used in this paper has the PWM timers with the triangular shape carrier waveforms.

There is $2\pi/3$ rad of phase-shift in each carrier. The each PWM timer can then generates interrupts on the peak or valley point of the carrier at every switching cycle. The current sampling and the controller iteration are conducted when each interrupt is generated. Fig. 8 illustrates the each phase's carrier, the interrupt instants, and the total operation sequence of the system with proposed reconstruction technique.

The operation sequence can be divided into four steps as shown in Fig. 8. If the interrupt instant is decided from

Fig. 8. Operation sequence of the proposed algorithm

the duty reference in the previous switching cycle, the reconstruction sequence is performed as follows.

- 1) The dc-link current is measured at the predetermined interrupt instant which can be either the peak or the valley point of the carrier.
- 2) Each phase current is reconstructed by measured the dc-link currents i_1 , i_2 , and i_3 during the interrupt period of the phase c carrier.
- 3) Each phase current is controlled with the digital current controller to balance out the phase currents. According to the direction of the current reference, the buck or the boost mode operation is determined.
- 4) The interrupt instant of the next period is decided with the duty reference of the controller.

The aforementioned operation sequence is periodically executed at every switching cycle. It should be noticed that the periodical iteration is a big advantage of the proposed method, because it can be easily implemented by software.

4. Simulation and Experimental Results

Simulation and tests were carried out to verify the proposed reconstruction method. The system parameters and the ratings are listed in Table 2.

4.1 Simulation results

PSIM 9.0 was used as the simulation tool. Fig. 9 compares the simulation waveforms of the actual and reconstructed phase current. Note that the proposed algorithm is very well performed so that the average current of each phase is accurately obtained.

Fig. 10 illustrates the simulation results of the transient response. In Fig. 10(a), the current reference is changed from 5A to 30A. After that, it is returned to its original value 5A again. In this case, the converter operates in buck

Fig. 9. Transient performance of the proposed method

Fig. 10. Simulation waveforms of the step response using type 3 digital current control and proposed reconstruction method. (a) Buck mode (b) Boost mode

mode. Similarly, the current reference is changed between -5A to -30A in Fig. 10(b) where the converter is under boost mode. To control the converter current, the designed type 3 current controller is used. As a result, the step response time of the phase currents is less than 50msec in buck mode and 70msec in boost mode. While the phase currents are controlled under the transient, each phase current is very well balanced.

4.2 Experimental results

A three-phase bidirectional interleaved dc-dc converter prototype was built for a battery charging application. The same system parameters introduced in Table 2 are used, and the proposed technique and the designed type 3 controller for the overall operation are implemented with Texas instrument's 32-bit floating point digital signal

controller TMS320F28335.

Fig. 11 shows the dc-link current and the phase currents with different duty references. It is verified that the dc-link current measured at the valley points of PWM is equal to each phase current when the output duty is less than 0.333 in Fig. 11(a). In Fig 11(b), the dc-link current is sampled at the peak points. At this time, the proposed reconstruction method should be adopted to reconstruct the phase currents because the measured current is not equal to individual phase currents. If the duty reference ranges between 0.333 and 0.666 as shown in Fig. 11(c), the dc-link current measured at the valley points has the direct information of the corresponding phase current, and the dc-link current measured at the peak points is the sum of two phase currents.

Accordingly, it is possible to measure at either the peak or the valley point for current reconstruction.

Fig. 12 represents the experimental waveform when the system operates under the non-reconstruction region, in case that the duty reference is placed between $(0.666-d_{mw})$ and $(0.666+d_{mw})$, and the current sampling is executed at the valley points. Here, d_{mw} was selected as 0.08 considering $2\mu s$ of the current reconstruction interval. At this time, the phase currents are not completely reconstructed as explained before. However, if the sampling point alters from the valley points to the peak points, the phase currents are well reconstructed.

(b)

(c)

Fig. 11. Phase currents and dc-link current (a) $d = 0.2$, (b) $d = 0.75$, (c) $d = 0.45$

Fig. 12. Non-reconstruction region under valley point sensing

(a)

(b)

Fig. 13. Experimental results of the step response using the type 3 digital current controller and the proposed reconstruction method: (a) operation as buck-mode; (b) operation as boost-mode

In order to show the dynamic characteristics of the converter, the step response results are shown in Fig. 13.

Fig. 13(a) shows the test waveforms under the reference current variation from 5A to 30A and 30A to 5A with the designed type 3 current controller in the buck-mode. The response time of the phase currents is less than 50msec at both variations, respectively.

Fig. 13(b) shows the test waveforms under reference current variation from -5A to -30A and -30A to -5A in the boost mode. As can be seen in the figure, the settling time of the phase currents is about 100msec at the step-up transition, and is nearly 150msec at the step-down transition. The difference with simulation seems caused by the parasitic elements.

5. Conclusion

In this paper, a new type of single current sensor technique for three-phase interleaved bidirectional converter has been proposed. The proposed method measures the dc-link current at either the peak or the valley point of the PWM carrier in regular, and the current reconstruction technique is applied to obtain each phase current information considering the duty reference and the non-reconstruction region.

The important results are summarized as follows:

- 1) The proposed current reconstruction scheme is possible to reduce the sensors and eliminate the scaling error that is caused by the multiple current sensors.
- 2) The proposed method has the non-reconstruction region only near the duty-ratio of 0 and 1. This result shows that the proposed method is useful in normal operation region without severe distortion.
- 3) The individual digital current controller of each phase is designed to balance the phase currents with the reconstructed currents.

The proposed method has been verified by the simulation and experimental results using the 3kW three-phase interleaved bidirectional converter.

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