Half Load-Cycle Worked Dual SEPIC Single-Stage Inverter

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Abstract – The two-stage inverter is widely used in traditional DC/AC inverter. It has several disadvantages such as complex topology, large volume and high loss. In order to overcome these shortcomings, a novel half load-cycle worked dual SEPIC single-stage inverter, which is based on the analysis of the relationship between input and output voltages of SEPIC converters operating in the discontinuous conduction mode (DCM), is presented in this paper. The traditional single-stage inverter has remarkable advantages in small and medium power applications, but it can’t realize boost DC/AC output directly. Besides one pre-boost DC/DC converter is needed between the DC source and the traditional single-stage inverter. A novel DC/AC inverter without pre-boost DC/DC converter, which is comprised of two SEPIC converters, is studied. The output of dual SEPIC converters is connected with anti-parallel and half load-cycle control is used to realize boost and buck DC/AC output directly and work properly, whatever the DC input voltage is higher or lower than the AC output voltage. The working principle, parameter selection and the control strategy of the inverters are analyzed in this paper. Simulation and experiment results verify the feasibility of the new inverter.

Keywords: SEPIC, SPWM, Single-stage inverter, Half load-cycle worked

1. Introduction

The two-stage inverter is composed of a high frequency pre-isolated DC/DC converter and a post-grid side inverter [1,2]. Restricted by natural conditions, the output power and output voltage of photovoltaic array fluctuate widely. The output voltage of photovoltaic array is generally lower than the peak voltage that occurs at the grid side. Therefore, it is necessary to increase the amplitude of the photovoltaic array output voltage through the boost converter to match the grid voltage [3, 4]. The addition of a boost converter is necessary, which adds complexity to the system structure, increases the size and weight of inverter and hampers the improvements of system efficiency. In recent years, the single-stage inverter has been widely used in photovoltaic system [5, 6]. Compared with the two-stage grid-connected photovoltaic inverter, the single-stage inverter can reduce the system complexity, save costs and improve reliability.

Two DC/DC converters are needed to implement the dual polarity DC/AC voltage because the output voltage of the basic DC/DC converter is unipolar. In recent years, single-stage inverters based on either the dual buck converter or the dual buck-boost converter have been proposed. All inverters are attributed to the combination structure of the DC/DC converter. The single-stage inverter mentioned above can be divided into serial connection and parallel connection [7]. Dual buck-boost inverter [8] and flyback inverters [9,10] belong to the serial combination. The input of dual buck-boost inverter is combined in parallel and the output is combined in serial. The output of isolation buck-boost converter used in flyback inverter is also connected in serial and the difference of both the output voltage is AC voltage needed. Because dual DC/DC converters work simultaneously and an isolation transformer is used in flyback inverter, the circuit loss of single-stage inverter with the output in serial combination is high and it is not conducive to improving conversion efficiency. Dual buck inverter [11, 12] and dual buck-boost inverter [13] belong to the parallel combination. Half load-cycle control is used, where each DC/DC converter only works in half-cycle and the output of each DC/DC converter is negative or positive, respectively. However, the dual buck inverter works in step-down mode and dual buck-boost inverter suffers from the polarity reversal problem.

SEPIC is one of the six basic DC/DC converters and it has more advantages than the others [14, 15]. SEPIC has several merits, including the capability of operating in both step-up and step-down modes, its input and output current is continuous, and output voltage is in phase with input voltage without suffering from the polarity reversal problem. These advantages have made SEPIC become a focus of power electronic application in recent years. Dual SEPIC single-stage inverter, which is comprised of two SEPIC converters and both the output are with anti-parallel connection, is presented in this paper [16, 17]. Half load-cycle control is used in dual SEPIC single-stage inverter, which is based on dual SEPIC. When half load-cycle worked dual SEPIC single-stage inverter works, its operating current is limited to a single SEPIC, which is...
helpful to improve conversion efficiency.

2. Working Principle of Dual SEPIC Single-stage Inverter

The main circuit topology of dual SEPIC single-stage inverter is shown in Fig. 1. The dual SEPIC single-stage inverter is comprised of positive unit and negative unit. The positive and negative units are SEPIC converters. The output of positive unit and negative unit are connected in anti-parallel. Switches S₁, S₂, S₃ and S₄ are full-controlled devices. Switches, S₁ and S₂, are used in positive unit. S₁ is used as selection switch of positive unit and S₁ is used to control positive half-cycle AC voltage output. Switches, S₃ and S₄, are used in negative unit. S₃ is used as selection switch of negative unit and S₄ is used to control negative half-cycle AC voltage output. As shown in Fig. 1, switch S₂ is ‘on’ and the positive SEPIC converter is selected. Switch S₁ is controlled by SPWM to achieve positive half-cycle AC output in the positive half-cycle. During the negative half-cycle, switch S₃ is ‘on’ and the negative SEPIC converter is selected, and switch S₄ is also controlled by SPWM to achieve negative half-cycle AC output.

SEPIC converter works in a higher power factor, has no problem of the transformer leakage inductance and changes to the isolation structure easily. These advantages listed above are conducive to improving power factor of dual SEPIC single-stage inverter and promoting its practical application.

To reduce the size and the cost of dual SEPIC single-stage inverter, the two inductors of positive and negative units can be wound on a magnetic core, respectively. In the area of photovoltaic power generation and battery-powered applications, the photovoltaic array and battery can be used as power supply of positive and negative units. Due to its characteristics of step-down and step-up, the output voltage is kept constant by adjusting the duty ratio of driving signal on S₁ and S₃, under the condition that the supply voltage amplitude difference between positive and negative units is remarkable.

Compared with the other DC/DC converter, the operation mode criterion of SEPIC converter is different and it is determined by the sum of the current through inductor L₁ and L₂. If the sum is still greater than zero, SEPIC works in continuous conduction mode (CCM), otherwise, in DCM. The operation mode which works in DCM is needed to achieve AC output voltage. The theoretical analysis is listed below. The working principle of the SEPIC used in positive unit and the negative unit is the same, and the working principle of the positive unit is treated in detail.

The conduction time of switch S₁ is α₁T; discharge time of inductor L₁ is α₁T, and T is switching period. The operation mode of SEPIC which works in DCM can be divided into three stages.

Stage 1[0≤t≤α₁T]: switch S₁ is ‘on’, and diode D₁ is ‘off’. E₁→L₁→S₁ and C₁→S₁→L₂ are the working circuit, respectively. Inductor L₁ is charged by the source, E₁, and inductor L₂ is charged by storage capacitor C₁. The operation mode of stage 1 is shown in Fig. 2(a).

Stage 2(α₁T<t≤(α₁+α₂)T]: switch S₁ is ‘on’ and diode D₁ is ‘off’. E₁→L₁→C₁→D₁→load (C₂, R and L) and L₂→D₁→load are the working circuit. During the stage 2, E₁ supplies to load and storage capacitor C₁. Inductor L₁ releases stored energy to the load and also to storage capacitor C₁. Storage capacitor C₁ releases stored energy to inductor L₂. The operation mode of stage 2 is shown in Fig. 2(b).

Stage 3[(α₁+α₂)T< t≤ T]: switch S₁ is ‘off’ and diode D₁ is ‘off’. The sum of the current through the

Fig. 1. Main circuit topology of dual SEPIC single-stage inverter

Fig. 2. DCM operating mode
inductor \( L_1 \) and \( L_2 \) is zero. \( E_s \rightarrow L_1 \rightarrow C_1 \rightarrow L_2 \) and \( C_2 \rightarrow \text{load} \) are the working circuit, respectively. During this stage, \( E_s \) supplies to storage capacitor \( C_1 \) and output capacitor \( C_2 \) supplies to the load. The operation mode of stage 3 is shown in Fig. 2(c).

### 3. Analysis and Parameter Calculation

The small ripple approximation is used in the steady-state analysis of SEPIC converter. Supposing that the capacity of capacitor \( C_1 \) and \( C_2 \) is large enough, though the input voltage \( E_1 \) and output voltage \( V \) are constant, respectively. When the SEPIC inverter works in DCM, the voltage across inductor \( L_1 \) is given by expression (1), and it is in comprised of three expression in a switching period, \( T \).

\[
v_{L1}(t) = \begin{cases} 
E_1 & (0 \leq t \leq \alpha_1 T) \\
-V & (\alpha_1 T \leq t \leq (\alpha_1 + \alpha_2) T) \\
0 & ((\alpha_1 + \alpha_2) T \leq t \leq T)
\end{cases}
\]  

(1)

Under the condition that the small ripple approximation is used and by the operating mode listed above, \( v_{L1}(t) \) is equal to \( v_{L2}(t) \). Supposing \( i_{L1}(t) = i_{L2}(t) \) and \( \frac{di_{L1}(t)}{dt} = v_{L1}(t)/L \), then the changing rage of \( i_{L1}(t) \) is given.

\[
\frac{di_{L1}(t)}{dt} = \frac{v_{L1}(t)}{L} + \frac{v_{L2}(t)}{L} = \frac{L_1 + L_2}{L_1 L_2} v_{L1}(t)
\]  

(2)

Substituting expression (1) into expression (2), the changing rage of inductor current of each stage is achieved. Concerning the analysis of operation mode listed above, waveforms of the current through inductor, \( i_{L1} \) and \( i_{L2} \), and diode, \( i_{D1} \), are shown in Fig. 3.

It can be seen from waveforms of the current through inductor, as shown in Fig. 3, that the peak value of \( i_{L1}(t) \), \( i_{pk} \), is equal to the product of changing rate of \( i_{L1}(t) \) and the time during the stage 1.

![Fig. 3. Waveforms of the current through inductor and diode](http://www.jeet.or.kr)

\[
i_{pk} = \frac{di_{L1}(t)}{dt} \alpha_1 T = \frac{L_1 + L_2}{L_1 L_2} E_s \alpha_1 T
\]  

(3)

According to the principle of inductor volt-second balance, expression (4) is given.

\[
E_s \alpha_1 T - V \alpha_2 T = 0 \Rightarrow \alpha_2 = \frac{E_s}{V} \alpha_1
\]  

(4)

Supposing the current through diode, \( i_{D1} \), is \( i_{D1}(t) \) and its average value is \( I_D \), \( i_{D1}(t) = i_{D1}(t) + V/R \) by the Kirchhoff’s current law. The steady-state average value of capacitor current is zero and average current through \( D_1 \) is obtained as

\[
I_D = \frac{V}{R}
\]  

(5)

According to the definition of the mean value, the average value of capacitor current is shown in expression (6). Expression (7) is achieved by integration of expression (6), which is equal to the area enclosed by the current. The expression of the average value of the current through diode is given in expression (8).

\[
I_D = \frac{1}{T} \int_0^T i_{D1}(t)dt
\]  

(6)

\[
\int_0^T i_{D1}(t)dt = \frac{1}{2} i_{pk} \alpha_2 T
\]  

(7)

\[
I_D = \frac{1}{T} \left( \frac{1}{2} i_{pk} \alpha_2 T \right) = \frac{i_{pk}}{2} \alpha_2
\]  

(8)

Solving the expression (5) and (8) and substituting expression (3) and (4) into them, expression (9) is achieved.

\[
\frac{V}{R} = \frac{1}{2} \frac{L_1 + L_2}{L_1 L_2} \frac{E_s^2}{V} \alpha_1^2 T
\]  

(9)

The voltage conversion ratio is listed as below.

\[
M(\alpha_1) = \frac{V}{E_s} = \frac{\sqrt{(L_1 + L_2)RT}}{2L_1 L_2} \alpha_1
\]  

(10)

It can be seen from the expression (10), the output voltage of SEPIC, \( V_s \), is proportional to the PWM pulse duty ratio, \( \alpha_1 \), when the SEPIC inverter works in DCM and in phase with input voltage, \( E_s \), without suffering from the polarity reversal problem. When the SEPIC inverter works in DCM, the PWM pulse duty ratio, \( \alpha_1 \), changes in accordance with the sinusoidal and the output voltage, \( V_s \), changes synchronously.

The steady-state critical condition of CCM and DCM is needed to make the dual SEPIC single-stage inverter work
in DCM by the selection of the inverter parameters. When SEPIC works in critical point between CCM and DCM, the current through inductor is in critical state of continuous or discontinuous and SEPIC operates in the first and second stages of DCM. The expression of voltage conversion ratio under CCM is shown in expression (11).

\[ M(\alpha_1) = \frac{\alpha_1}{1-\alpha_1} \quad (11) \]

Assuming the average value of current through inductor is \( I_L \), the current through output capacitor, \( C_2 \), is given.

\[ i_{c2}(t) = \begin{cases} \frac{V}{R} (0 \leq t \leq \alpha_1 T) \\ I_L - \frac{V}{R} (\alpha_1 T < t \leq T) \end{cases} \quad (12) \]

According to the principle of steady-state capacitor ampere-second balance, expression (13) is achieved.

\[ \int_0^T i_c(t) dt = \frac{V}{R} \alpha_1 T + (I_L - \frac{V}{R}) (1-\alpha_1) T = 0 \quad (13) \]

Expression (14) is obtained by solving expression (13).

\[ I_L = \frac{V}{(1-\alpha_1) R} = \frac{\alpha_1 E_1}{(1-\alpha_1) \alpha} R \quad (14) \]

As the waveforms of the current through inductor shown in Fig.3, expression (15) is needed to make the inductor current intermittent.

\[ I_L < I_{pk} / 2 \quad (15) \]

Substituting expression (3) and expression (14) into expression (15), expression (16) is achieved.

\[ \frac{\alpha_1 E_1}{(1-\alpha_1)^2 R} < \frac{L_1 + L_2}{2L_1 L_2} E_1 \alpha_1 T \quad (16) \]

Solving expression (16), expression (17) is given.

\[ \alpha_1 < 1 - \frac{2L_1 L_2}{(L_1 + L_2) RT} \quad (17) \]

Expression (17) is the operation condition of SEPIC working in DCM. Under the condition that the load and circuit parameters are determined and \( \alpha_1 \) meets the expression (17), the SEPIC works in DCM and the output voltage of SEPIC, \( V \), is proportional to \( \alpha_1 \). When the switches \( S_1 \) and \( S_3 \) are controlled according to pwm law, \( \alpha_1 \) changes with pwm law and the maximum value of \( \alpha_1 \) is modulation index of pwm, \( M \). As long as \( M < \text{MAX}(\alpha_1) \), AC sinusoidal output voltage is achieved.

To make sure that SEPIC works in DCM within the limitation of modulation index, \( M \), circuit parameters should be selected according to expression (10) and expression (17), and voltage conversion ratio should be considered too.

Load Resistance \( R=10 \Omega \), maximum duty ratio, \( \alpha_{\text{max}} \), is 0.5. The voltage conversion ratio \( M(\alpha) \geq 2 \). Frequency of triangular ‘carrier’ wave is 12kHz.

Assuming \( L_1 = L_2 \), according to expression (10) can be obtained that \( L_1 = L_2 < 52 \mu H \), \( L_1 = L_2 = 40 \mu H \) is used and \( M(\alpha_{\text{max}}) = 2.28 > 2 \). It is also verified by expression (17) and the maximum duty ratio \( \alpha_{\text{max}} = 0.5 < 0.78 \).

\( E_1 = E_2 = 24V \). Maximum peak voltage is 54V and rms voltage, \( V_o \), is 38V. The output capacitor is used to filter out high-order harmonic component. The greater the output capacitor, the better the filter and the larger the current through the output capacitor \( C_2 \). Generally, current through output capacitor is less than 50% \( I_o \).

According to expression (18),

\[ I_{C2} = C_2 \frac{dv_o}{dt} \Rightarrow C_2 \leq \frac{I_{C2}}{V_o \omega_o} = \frac{1.9}{38 \times 50 \times 2\pi} \quad (18) \]

The output capacitor is obtained, \( C_2 < 159 \mu F \) and \( C_2 = 40 \mu F \) is used.

Storage capacitor \( C_1 \) is used for energy storage and release. During the period of the switch is ‘on’, the fluctuation voltage across \( C_1 \) is

\[ \Delta V_{C1} = \sqrt{\frac{(L_1 + L_2) R T}{2L_1 L_2} \frac{V_o \alpha_1^2 T}{C_1 R}} \quad (19) \]

Supposing that \( \Delta V_{C1} / V_{C1} < 0.1 \), \( \alpha_{\text{max}} \) is 0.5 and \( C_1 \) is obtained as \( C_1 > 8.33 \mu F \). \( C_1 = 20 \mu F \) is used.

### 4. Control Scheme of Dual SEPIC Single-stage Inverter

In order to ensure that the output voltage of the dual SEPIC single-stage inverter is sinusoidal, the system control scheme in Fig. 4 is used. Half load-cycle control is used to ensure positive and negative unit work alternately. Switches \( S_1 \) and \( S_3 \) work according to unipolar SPWM law, and the driving signal of \( S_1 \) is achieved by comparing positive half-cycle of sine wave, \( V_{\text{ref}} \), with the positive triangular ‘carrier’ wave, and the driving signal of \( S_3 \) is achieved by comparing reversal negative half-cycle of sine wave, \( V_{\text{ref}} \), with the positive triangular ‘carrier’ wave. \( S_2 \) and \( S_4 \) work alternately, \( S_1 \) is ‘on’ in positive half-cycle and \( S_3 \) is ‘on’ in negative half-cycle. The dead-band delay
between $S_2$ and $S_4$ is needed to prevent shoot-through between the two output capacitors $C_2$ and $C_4$. The output voltage of positive half-cycle and output voltage of negative half-cycle are controlled by positive and negative unit, respectively.

It should be noted that when the unipolar SPWM is used, modulation ratio, $M$, should be limited to ensure positive/negative unit of inverter work in DCM. Once the converter works in CCM, the inverter does not work properly according to the sine law which causes the output voltage to distort.

5. Simulation Results based on PSIM

In this paper, simulation model of dual SEPIC single-stage inverter is built using PSIM. The simulation parameters are listed as below. DC source $E_1=E_2=24V$. Storage capacitor $C_1=C_3=20\mu F$ and output capacitor $C_2=C_4=40\mu F$. Inductor, $L_1=L_2=L_3=L_4=40\mu H$. Resitive load is used, load resistance $R=10\Omega$. Frequency of triangular ‘carrier’ is 12kHz. Frequency of sinusoidal reference waveform is 50Hz. Modulation index is 0.5 and MOSFET is used.

According to expression (17), when $\alpha_1 \in [0,0.78]$, the inverter works in DCM and modulation index $M=0.5$ is included.

The simulation results are shown in Fig. 5. Fig. 5(a) and Fig. 5(b) show current through inductor, $i_{L1}$ and $i_{L2}$, and current through diode, $i_{D2}$. It can be observed from Fig. 5(a) and Fig. 5(b) that current through inductor is consistent with the theoretical analysis. Fig. 5(b) also demonstrates the DCM operating mode. Fig. 5(c) shows current through inductor, $i_{L1}$ and $i_{L2}$, and output voltage of inverter, $V_o$. Fig. 5(d) shows voltage across storage capacitor, $V_{C1}$ and output capacitor, $V_{C2}$, and output voltage of inverter, $V_e$. It is clear from Fig. 5(c) and Fig. 5(d) that the two SEPIC converter work in alternate half load-cycle worked as studied in this paper and operate in both step-up and step-down modes. In a word, the simulation results reveal that a single-stage boost inverter can be achieved using dual SEPIC single-stage inverter and shows a good agreement with the analysis above.

6. Experiment Results

A prototype is implemented to validate the feasibility of the dual SEPIC single-stage inverter. The TMS320F2812 digital signal controller is used for control strategy. The circuit parameters are consistent with the simulation parameters. MOSFET IRF740 and fast recovery diode MUR8100E series combination are used as unidirectional switch $S_1$ and $S_3$ to meet with the input voltage of 24V. Switch $S_2$ and switch $S_4$ are MOSFET IRF740. A digital storage oscilloscope is used to record experiment waveform. The experiment results of dual SEPIC single-stage inverter with resistive load are depicted in Fig. 6. Current through inductor, $i_{L1}$ and $i_{L2}$ and diode, $i_{D1}$, are shown in Fig. 6(a). The waveforms of current through inductor ($i_{L1}$ and
i_{12} and diode (i_{01}) during a few switching periods are depicted in Fig. 6(b), which correctly demonstrates the DCM operating mode. Fig. 6(c) depicts current through inductor, i_{L1} and i_{L2}, and output voltage of inverter, v_o. Fig. 6(d) shows voltage across storage capacitor, v_{C1}, and output capacitor, v_{C2}, and output voltage of inverter, v_o. It is evident from Fig. 6(c) and Fig. 6(d) that half load-cycle worked dual SEPIC single-stage inverter works properly and the predicted AC voltage output is obtained. A very good agreement can be seen between simulation and experimental results.

![Fig. 6. Experiment results](image)

The efficiency curve of dual buck inverter [12], dual SEPIC inverter, dual buck-boost inverter [13], and flyback inverter [10] are shown in Fig. 7. It can be found that the efficiency of dual buck inverter is the highest. However, compared with both dual SEPIC inverter and dual buck-boost inverter, dual buck inverter only operates in step down mode, hence limiting the flexibility of the output voltage. On the other hand, the efficiency of flyback inverter is the lowest. It is caused by isolation transformer used in flyback inverter and full load-cycle operating mode of flyback inverters. Although the efficiency of both dual SEPIC inverters and dual buck-boost inverter is lower than that of dual buck inverter, these two kinds of inverters can operate in step-up and step-down modes, and alternately half load-cycle. Moreover, it can be found from Fig.7 that the efficiency of dual SEPIC inverter is higher than that of dual buck-boost inverter. It should be noted that the dual SEPIC inverter eliminate the polarity reversal problem which exists in dual buck-boost inverter.

**7. Conclusion**

A novel dual SEPIC single-stage inverter has been presented and analyzed. The proposed single-stage inverter is derived from the relationship between the input voltage and output voltage of SEPIC converter which operates in DCM. The output of both SEPIC is connected with anti-parallel. The half load-cycle control is used successfully in dual SEPIC single-stage inverter. The AC output voltage is good. Simulation model of dual SEPIC single-stage inverter using PSIM was established. Finally, a prototype of the inverter using TMS320F2812 was developed. The experimental and simulation results verify the feasibility of the inverter and the correctness of theoretical analysis.

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