Modeling and Experimental Validation of 5-level Hybrid H-bridge Multilevel Inverter Fed DTC-IM Drive

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Abstract – This paper aims to improve the performance of conventional direct torque control (DTC) drives proposed by Takahashi by extending the idea for 5-level inverter. Hybrid cascaded H-bridge topology is used to achieve inverter voltage vector composed of 5-level of voltage. Although DTC is very popular for its simplicity but it suffers from some disadvantages like- high torque ripple and uncontrollable switching frequency. To compensate these shortcomings conventional DTC strategy is modified for five levels voltage source inverter (VSI). Multilevel hysteresis controller for both flux and torque is used. Optimal voltage vector selection from precise lookup table utilizing 12 sector, 9 torque level and 4 flux level is proposed to improve DTC performance. These voltage references are produced utilizing a hybrid cascaded H-bridge multilevel inverter, where inverter each phase can be realized using multiple dc source. Fuel cells, car batteries or ultra-capacitor are normally the choice of required dc source. Simulation results shows that the DTC drive performance is considerably improved in terms of lower torque and flux ripple and less THD. These have been experimentally evaluated and compared with the basic DTC developed by Takahashi.

Keywords: DTC, Multilevel inverter, Induction motor, VSI.

1. Introduction

Direct torque control (DTC) induction motor drive is becoming more popular day by day due to its fast dynamic response and robustness to the variation of the machine parameters without using the current controller [1-6]. Implementation of this control strategy is very simple and also coordinate transformation is not required. It is one of the most efficient control method for induction motor (IM) since its invention [7]. Performance superiority and control simplicity made DTC drive one of the prominent research areas in IM drives system. But most of the above-mentioned advantages come with the cost of high torque and flux ripple.

However, the high torque ripple problem allied with the basic DTC system can be reduced by efficiently increasing the output resolution of the inverter. Many methods have already been introduced to address this problem such as zero state modulation [8, 9], space vector modulation (SVM) [2, 8, 10, 11] and the application of multilevel inverter [4, 5, 12-17]. These modified schemes generally provide better performance in terms of torque and flux smoothing with added switching losses and power circuit complexity.

Therefore, modified inverter circuit is introduced recently

for IM-DTC drives. Innovative switching table with four level hysteresis controllers for flux and torque is proposed in [18] to construct a three-level inverter. Comparison shows a significant improvement in terms of harmonic and switching frequency over its ancestor two level inverter. The torque ripple problem associated with the hysteresis controller and look-up based switching signal generator is solved with PI controller and the SVM inverter [19]. The SVM-DTC drive imitates the advantages of basic DTC with torque and flux ripples minimization, but it requires powerful processor and runs at higher switching frequency.

It is reported in the literature that matrix converter is used replacing rectifier-inverter [11]. IM-DTC drive based on matrix converter is applied in two different modes, namely, basic DTC and SVM-DTC and the results have shown that it can maintain unity power factor at the supply side.

In other study proposed for DTC control scheme fed by multilevel inverter utilize the SVM [10] and predictive control strategy [20] for selecting the voltage vector rather than look-up table. Significant improvement of flux ripple as well as torque ripple is reported. But the uses of mathematically complex equations require processor with high computational power, particularly if the voltage levels are high [14]. For this drawback some researchers preferred to use look-up table based switching signal [21-23]. Advantage of these approaches is simplicity yet good dynamic responses.

However, the application of multilevel inverter improves the ST-DTC (Switching table based direct torque control) performance providing flexibility of choosing the required voltage vector from higher number of available voltage

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vectors compared to basic two level DTC. Three main multilevel inverter topologies have been found in industrial application; flying capacitors (FC) [24], cascaded H-bridge (CHB) [5, 10, 25] and neutral point clamped (NPC) [26, 27]. Simple design and modular structure of cascaded H-bridge multilevel inverter has the inherent advantages among these inverter topologies. With “c” H-bridge cells in each arm, maximum possible number of levels by an inverter is $3c$ and it can be generated when the dc supply voltages of the cascaded cells are chosen by ratio three [28].

Multilevel inverters with promising advantages require higher number of switches and isolated dc supply for each cell. As a result price of the drives increases and the reliability decreases. In this work, number of switch has been reduced by replacing three H-bridge cell with a single six switch inverter keeping the same number of voltage vector proposed in [5, 10]. Section 2 shows the hybrid topology that is proposed in this work. Another problem of ST-DTC with MLI is the requirement of high sampling rate to utilize the inherent advantage of the inverter. Therefore, the control algorithm should be optimized to converge within the sampling period. In this article, empirical equation is introduced to address this problem. It is explained in section 5.2.

High acceptability of DTC-IM drives lies on its simple control strategy. But unfortunately complexity highly increases when the number of voltage vector goes high. In this work a simple graphical presentation of the vector selection table is introduced to explain how the switching state could be selected from the switching table. It cannot be guaranteed that the switching sequence that is employed in [5] is optimized but the graphical presentation of the vector selection table employed in this work can provide an intuitive knowledge to optimize the switching strategy for future investigation.

In the following section, concept of multilevel inverter is introduced. Section 3 graphically illustrates the voltage vectors and inverter state, followed by a brief description on the fundamental concept of DTC in section 4. Section 5 describes the control strategy of proposed DTC scheme. Simulation results and discussion is presented in section 6, followed by an implementation in section 7 and finally section 8 concludes the paper.

2. Hybrid Cascaded H-bridge MLI

Cascaded H-bridged cell is one of the basic topology of multilevel inverter (MLI). Advantage of this structure is its modular structure where the inverter contains small identical cell. But it requires high number of isolated dc supply. k -cell in each arm of inverter has $(2k+1)$ voltage level and it needs $3k$ isolated dc supply. In the proposed method, high voltage stage is replaced with standard six switch topology and hence it reduces the total number of dc supply by 2. As a result required number of dc supply

Fig. 1. 5-level hybrid cascaded H-bridge multilevel inverter feeding induction motor.

becomes $3k-2$.

It is reported that number of voltage level can be increased adopting asymmetrical source [29]. Difference in individual cell voltage produces higher number of voltage step and therefore higher number of levels for same circuit topology. Maximum number of uniform step can be achieved when the cells are supplied by a voltage of ratio three [30].

Study shows that the appropriate voltage ratio which satisfied the modulation condition to avoid high frequency operation at high-voltage level if two adjacent voltage levels are realized only selecting the lowest voltage cell. But this condition does not satisfy for ratio three based topology. Nevertheless this ratio is selected for some topology where PWM control is not applied. This problem has also been addressed in [16].

Structure of the five level cascaded hybrid bridge multilevel inverter (CHBMLI) introduced in this paper is shown in Fig. 1. High voltage stage is consisting of conventional six switch inverter and each of its phases is connected in series with H-bridge medium voltage stage. High voltage stage is supplied by only one dc supply whereas medium voltage stage is supplied by 3 isolated dc supply. Compared to asymmetrical MLI, one dc supply is used in place of 3 isolated dc supplies. Additionally, in asymmetrical MLI, ability of bidirectional current sourcing is required for the three high-voltage-stage supplies except the load power factor is constantly close to unity. In this proposed design, bidirectional current capability is not necessary unless the load is operating in regenerative mode. Medium voltage supply is identical with those of asymmetrical MLI but owing to the lower voltage levels cost of the stage is much lower compared to the main high voltage stage. As a result significant reduction of dc supply cost can be achieved by this topology [3].

To determine the output voltage levels of used topology in Fig. 1, any output phase (A, B or C) voltage with respect

to negative terminal of high voltage stage is considered. Therefore output voltage levels varies in between $(3+1)V_s = 4V_s$ to $(0-1)V_s = -1V_s$ with uniform stepping of V_s . Thus it forms a 5-level inverter.

3. Voltage Vectors and inverter states

Switching variables of the MLI represented by $[X_{abc}, Y_{abc}]$ where X is (0 or 1) whereas Y is (-1, 0 and +1). States of the high and medium stages are determined by X_{abc} and Y_{abc} respectively. Output voltage vector can be calculated using following Eq. (1) where V_{ab}, V_{bc}, V_{ca} represent line to line voltage and V_{an}, V_{bn}, V_{cn} represent phase voltage.

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = 3V_s \begin{bmatrix} X_a - X_b \\ X_b - X_c \\ X_c - X_a \end{bmatrix} + V_s \begin{bmatrix} Y_a - Y_b \\ Y_b - Y_c \\ Y_c - Y_a \end{bmatrix} \quad (1)$$

Phase voltages of the Y-connected load is represented by the following Eq. (2)

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} V_{ab} - V_{ca} \\ V_{bc} - V_{ab} \\ V_{ca} - V_{bc} \end{bmatrix} = \frac{V_s}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 3X_a + Y_a \\ 3X_b + Y_b \\ 3X_c + Y_c \end{bmatrix} \quad (2)$$

The voltage vector realized by Park's transformation is given in (3)

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (3)$$

Substituting (2) into (3) gives

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = V_s \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} 3X_a + Y_a \\ 3X_b + Y_b \\ 3X_c + Y_c \end{bmatrix} \quad (4)$$

Eq. (4) can be used to generate any voltage vector from any inverter switching state. Voltage vector diagram for 5 levels inverter can be drawn by superposition of individual stage vector diagram. First, vector diagram of the two-level inverter (high voltage stage) is drawn. Then on each tip of the vectors including zero vectors (center) a complete vector diagram of medium stage is super imposed. Fig. 2(a) and 2(b) represent the voltage vector of high voltage stage and medium respectively. The final vector diagram is shown in Fig. 2(c). There are 5^3 phase voltage combination is possible for 5-level inverter with $(L-1)+1=61$ unique voltage vector. Number of the inverter levels is represented by ' L '. Therefore the number of voltage vector generated by a multilevel inverter is higher if the inverter topology offers higher number of voltage level. It gives more degree of choice to select the desired voltage vector for control purpose. Voltage vector produced by a 5-level

Fig. 2. (a) voltage vectors of medium stage (b) Voltage vector of high voltage stage (c) 5-level inverter voltage vector diagram.

hybrid CHBMLI is shown in Fig. 2(c). Each vector is drawn along with its switching state. For medium stage first two digits represent phase 'A' upper switch S_1 and S_3 . Similarly, next two digits stand for phase 'B' and last two digits for phase 'C'. For high state, first digits stand for phase 'A' and goes respectively for other two phase.

4. Fundamental Concept of DTC

Configuration of the basic DTC proposed by Takahashi and Noguchi [1] is illustrated in Fig. 3. In this method measured terminal variables are utilized to estimate instantaneous value of the flux and torque. From the estimated value of flux and torque an optimal switching vector is selected to directly control the torque.

Any voltage applied to the IM can be represented in stationary reference frame with the following equation:

$$v_s = R_s i_s + d\psi_s/dt \quad (6)$$

It can be assumed that for a small time difference Δt resistive drop across the stator is very small and can be neglected. Therefore Eq. (6) can be rewritten as:

Fig. 3. Basic DTC block diagram

Fig. 4. Rotation of the stator flux linkage.

$$\Delta\psi_s = v_s \Delta \quad (7)$$

Eq. (7) clearly indicates that the stator flux vector ψ_s directly following the change of the stator voltage vector. Therefore selecting the appropriate voltage vector can effectively control the stator flux locus. It is shown in Fig. 4. Where $\psi_s|_{t=0}$ is the initial flux linkage at the instant of switching.

However, the only drawback for this control is the staggered motion of the rotor due to the use of voltage vector fed by VSI. Stator-rotor flux angle related with the torque can be written as:

$$T_e = \frac{3}{2} P \psi_s \times i_s = \frac{3}{2} P |\psi_s| |\psi_r| \sin \theta_{sr} \quad (8)$$

Where, $|\psi_s|$ represent the degrees of stator flux linkage and $|\psi_r|$ represent the rotor flux linkage. Stationary reference frame is considered to represent Eq. (8). Motion profile of the rotor flux is smoother than its creator stator flux and it rotates behind the rotor flux in lagging manner. This produces the leakage reactance of the rotor and stator. Fortunately as a result of that, vibrating motion of the stator flux is filtered out from its follower rotor flux. When the voltage vector is applied to the stator, instantly it creates a rotating flux. This flux rotates leaving the rotor flux behind which produce the angle between the fluxes. Therefore this angle can be controlled applying the proper voltage vector. As a result of that torque of the motor can be controlled.

In short, amplitude of the stator flux is proportional to applied voltage vector across rotor terminal which control the amplitude of the rotor flux and its rotation. Thus produces the angle between them which can be controlled effectively to manipulate the torque. This idea is used in DTC drive to achieve required torque and flux response in induction machine.

5. DTC with Hybrid Asymmetric MLI

In basic DTC scheme appropriate voltage vector is selected from the 2-level inverter. But this inverter, however, is limited to offer few number of voltage vectors irrespective to the torque demand. There by same voltage vector is selected for large and small torque and the flux error. Options of selecting the voltage vector can be greatly enhanced by 5-level asymmetrical MLI as the number of available voltage vector is high. It offers more degree of freedom to select proper voltage vector to regulated torque and flux. Thus the dynamic behavior of torque and flux is improved. Fig. 5 shows the block diagram of proposed DTC scheme.

Fig. 5. Block diagram of proposed DTC scheme.

5.1 Vector selection strategy for the proposed DTC

Torque can be controlled by retaining constant stator flux and speeding up the rotation of the flux linkage as quickly as possible. Amplitude and rotation of the stator flux can be maintained constant by selecting proper inverter voltage vectors. Inverter voltage vector can be defined as:

$$v_s = v_{an} + v_{bn} e^{j(2/3)\pi} + v_{cn} e^{j(4/3)\pi} \quad (9.a)$$

$$v_s = [1 \quad e^{j(2/3)\pi} \quad e^{j(4/3)\pi}] [v_{an} \quad v_{bn} \quad v_{cn}]^T \quad (9.b)$$

Using Eq. (2) and after algebraic manipulation it becomes as follows:

$$v_s = \frac{v_s}{3} \begin{bmatrix} 1 \\ e^{j(2/3)\pi} \\ e^{j(4/3)\pi} \end{bmatrix}^T \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 3X_a + Y_a \\ 3X_b + Y_b \\ 3X_c + Y_c \end{bmatrix} \quad (9.c)$$

Table 1. Switching table of phase ‘A’

S13	S1	S3	X _a	Y _a	Output
0	0	0	0	0	0
0	1	0	1	0	V _s
0	0	1	-1	0	-V _s
0	1	1	0	0	0
1	0	0	0	1	3V _s
1	1	0	1	1	4V _s
1	0	1	-1	1	2V _s
1	1	1	0	1	3V _s

When the stator winding is fed by an inverter as shown in Fig. 1, voltage v_{an} can be determined by the state of the switches (S1, S2, S3 and S4) of medium stage phase and high stage switches (S13 and S14). Similarly the voltage v_{bn} and v_{cn} can be determined from the state of their respective switches. Phase ‘A’ of medium stage full bridge consists of switches S1, S2, S3 and S4 and connected to dc voltage V_s . High voltage stage of the inverter is a conventional six switch (S13...S16) inverter and supplied by $3V_s$. Each arm of the six switch inverter is cascaded with corresponding phase of the medium stage. Switching state and output voltage of phase ‘A’ of this topology is shown in Table 1. State of S2, S4 and S14 are skipped as they are always complimentary to S1, S3 and S13 respectively to avoid short-circuit of dc source. For phase ‘B’ and ‘C’ similar switching table can be constructed.

Eq. (9.c) is expressed in terms of switching variable $X_a, X_b \dots Y_c$. However, these variables can be further represented as function of switching state as follows:

$$\begin{aligned}
 X_a(S_{13}) &\in \{0,1\} \Rightarrow X_a(S_{13}) = S_{13} \\
 X_b(S_{15}) &\in \{0,1\} \Rightarrow X_b(S_{15}) = S_{15} \\
 X_c(S_{17}) &\in \{0,1\} \Rightarrow X_c(S_{17}) = S_{17} \\
 Y_a(S_1, S_3) &\in \{-1,0,1\} \Rightarrow Y_a(S_1, S_3) = S_1 - S_3 \\
 Y_b(S_5, S_7) &\in \{-1,0,1\} \Rightarrow Y_b(S_5, S_7) = S_5 - S_7 \\
 Y_c(S_9, S_{11}) &\in \{-1,0,1\} \Rightarrow Y_c(S_9, S_{11}) = S_9 - S_{11}
 \end{aligned}$$

Where $S_N \in \{0,1\}$

Therefore Eq. (9.c) can be represent as

$$\begin{aligned}
 v_s(S_1, S_3 \dots S_{17}) &= \\
 \frac{V_s}{3} \begin{bmatrix} 1 \\ e^{j(2/3)\pi} \\ e^{j(4/3)\pi} \end{bmatrix}^T \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 3S_{13} + S_1 - S_3 \\ 3S_{15} + S_5 - S_7 \\ 3S_{17} + S_9 - S_{11} \end{bmatrix} \quad (10)
 \end{aligned}$$

Using Eq. (10) any voltage vector can be calculated if the switching states are known. Combined switching vector along with their switching state has already been shown in 2(c).

However, to select the desired voltage vector it is labeled as shown in Fig. 6(a) and thereby a look up table is constructed. Fig. 6(b) is the zoomed version of the shaded triangle in Fig. 6(a). It shows that that the vector 8 can be achieved by three different switching states. This redundancy actually opens up a scope to optimize the

Fig. 6. (a) Labeled vector diagram of proposed MLI; (b) Zoomed version of shaded triangle

switching frequency of high voltage stage and switching losses. However to optimize the switching losses a technique proposed [31] is adopted.

5.2 Flux and torque control Strategy

With several choices in hand to select the desired voltage vector, a proper selection scheme must be adopted to achieve the desired dynamic torque response and to keep the switching loss as low as possible. It is mentioned in previous section, 5-level inverter offers 61 useable voltage vectors. Therefore the d-q plane of the voltage vector is subdivided into 12 sectors with 30° of each started from -

15°. Empirical rules is used and investigation shows that a 4 level torque hysteresis along with 9 level torque hysteresis utilize the highest number of available voltage vector in d-q plane. It is due to the fact that as the number of sector goes high in the worst case scenario 2N comparison is need to achieve solution for the sector. Where, N is the number of sector in vector space. Whereas, using the empirical equation need only one comparison to select the necessary equation to find the sector. Sector is calculated using following set of equations.

$$\theta = \arctan\left(\frac{\Psi_y}{\Psi_x}\right) \quad (11.a)$$

$$N = \begin{cases} \text{FLOOR}\left(\frac{\theta}{30} + 0.5\right) - 15^\circ \leq \theta < 180^\circ \\ \text{FLOOR}\left(\frac{\theta}{30} + 12.5\right) - 15^\circ > \theta > -180^\circ \end{cases} \quad (11.b)$$

Where Ψ_x and Ψ_y are the real and imaginary component of estimated flux respectively. θ is the angle of rotating flux in d-q plane.

For any sector, estimated flux is compared with its nominal value and flux error (Ψ_{err}) is determined. In similar way torque error signal (T_{err}) is generated by comparing to its reference value. Both error signals are processed through its respective hysteresis controller to generate the index of 3D look-up table consist of 61 possible voltage vector. Flux and torque hysteresis controller is designed using the rule shown in Fig. 7. For flux hysteresis shown in Fig. 7(a), 5% of the nominal flux is taken as the hysteresis band. In the case of torque hysteresis shown in Fig. 7(b), 10% of the nominal torque is taken for the torque hysteresis band.

Using the above indexes generated by the hysteresis comparator along with sector number a predefined voltage vector is selected. The simple presentation of how the switching state could be selected from the switching table based on torque and flux demand is shown in Fig. 7(c) (shaded triangle, sector 1). For a positive torque demand vector situated above the sector boundary (shaded triangle) is used and for negative vectors below the sector boundary is selected.

- Each group of vectors connected by thick lines represents a particular flux demand.
- The higher the absolute value of the torque the far the vector goes from the sector boundary (creating the higher load angle). e.g. 38<39<40<41
- For higher flux demand vectors with higher amplitude are selected. e.g. 41-40-39-38, 60-59-58-57 for maximum positive flux and 11-10-2-0-6-16-15 for zero flux whereas 45-44-43-23, 33-55-54-53 for maximum negative.

A similar strategy can be drawn for even sector shown in Fig. 7(d) (shaded triangle, sector 2)

Fig. 7. (a) Five level hysteresis for flux controller (b) Nine level hysteresis for torque controller (c) Vector selection of sector -1 (Shaded Triangle (-15° to +15°)) (d) Voltage vector selection of sector -2 (Shaded Triangle)

6. Simulation

Simulation is done using MATLAB/Simulink. Parameters and rating used for the simulation and experimental

validation of IM is listed in Table 2. Both for conventional and proposed DTC scheme, same parameters are used.

Bandwidth of the stator flux controller is set to $\pm 5\%$ of the reference stator flux which is ± 0.1 Wb. For torque controller a hysteresis band of ± 0.9 Nm is selected. Flux and torque hysteresis controller is sub-divided according to Fig. 7(a) and 7(b) respectively. The dc-bus voltage is

selected to 400V dc for the case of basic DTC and for its multilevel counterpart the high voltage stage dc-bus voltage is kept to 300V dc whereas medium stage is one third of its high voltage stage.

Fig. 8 represent the steady state characteristics of the IM drive under the proposed control scheme. The mechanical speed is kept to $\Omega=50$ rad/s and load torque, $T_l=1$ Nm is

Fig. 8. Simulation result based on proposed MLI based DTC: (a) Stator current; (b) Stator PHASE VOLTAGE; (c) Stator flux; (d) Torque ripple

Fig. 9. Simulation result based basic DTC: (a) Stator current; (b) Stator phase voltage; (c) Torque ripple; (d) Stator Flux; (e) Sector succession

applied. Stator three-phase current and voltage (phase-A) are shown in Fig. 8(a) and 8(b) whereas Fig. 8(c) and 8(d) representing the stator flux ripple and the electromagnetic torque respectively. Zoomed part of the Fig. 8(b) clearly shows the voltage level. A zoomed look at Fig. 8(c) and 8(d) highlight the demagnetizing effect that appears repetitively at the beginning of each even sector which then over compensated in the next sector. As a result a small spike in both flux and torque appeared with an interval of two sectors.

Fig. 9(a)-(e) consecutively represent the phase current, phase voltage, torque ripple, flux ripple and sector succession, when basic DTC scheme is applied. From Fig. 8 and 9, it is evident that the proposed system outperforms in terms of flux and torque ripple to its counterpart of conventional DTC scheme.

Selection of the voltage vector in the proposed DTC scheme solely depends on the torque error and flux error. These means the gradient of the torque ripple (or flux) depend on the magnitude error of the torque ripple (or flux). Therefore the probability of overextend outside the hysteresis band for the torque is reduced.

Fig. 9(c) shows the torque response of conventional DTC using six switch inverter. The torque ripple band in this case is about 1.12 N-m. Fig. 8(d) is the torque response of proposed MLI version of DTC. In this instant the torque ripple is 0.34 N-m. Therefore using this topology and control about 70% torque ripple is reduced. In both case the load torque and speed demand is kept same.

Fig. 10. THD analysis of basic DTC at speed 500rpm

Fig. 11. THD analysis of proposed DTC at speed 500rpm

Fig. 12. Quantitative result in terms of torque (N-m) and flux ripple (Wb) and percentage THD of stator current.

Table 2. Parameters and rating used for the simulation and experimental validation

Parameter	Value	Parameter	Value
Power (kW)	0.9	Rotor Resistance (Ω)	22.63
Voltage (V)	380/660	Stator Inductance (H)	0.0563
Frequency (Hz)	50	Rotor Inductance (H)	0.0846
Pole Pair	2	Magnetizing Inductance (H)	0.9963
Stator Resistance (Ω)	21	Rated Speed (rpm)	1400

FFT analysis of the stator current for both proposed DTC and convention DTC is performed and shown in Fig. 8 and 9 respectively. THD has been calculated manually by considering only the first 50 harmonics. A comparative study in terms of torque (N-m), flux (Wb) and THD (%) is shown in Fig. 10 and found that a significant improvement is achieved in all the parameters.

7. Experimental Validation

An experimental validation is carried out using dSPACE (DS1104) powered with onboard DSP (TMS320F240). dSPACE comes with a software named controlled desk which facilitate an easy communication between MATLAB and onboard DSP. High voltage stage is implemented using SEMIKRON six-switch inverter. Medium voltage level is realized with 30A MOSFET. Four isolated dc sources are used to supply the inverter.

Fig. 13 represents the steady state behavior of phase current for an induction motor driven by conventional DTC strategy with six switch inverter. Fig. 14 shows the phase current of DTC-IM using proposed multilevel inverter and DTC strategy. Fig. 15 shows the phase (A) voltage of proposed DTC. The sampling period T_s is fixed to 0.1ms in both cases.

Figs. 16 and 17 respectively representing the torque ripple in conventional and proposed method which closely replicates the discussion carried out in simulation. Fig. 18 showing experimental setup used to verify the simulation of proposed method.

One of the important issue of the power converters and drives are its switching losses. It is calculated using Eq. (12) and the result are tabulated in Table 3.

$$P_{cond} = I_{on(rms)}^2 R_{ds,on} \quad (12.a)$$

Fig. 13. Phase current in conventional DTC

Table 3. Switching losses

Voltage Stage	No. of Switch	Average switching frequency (Hz)	Conduction loss (W)	Switching Transition loss (W)	Parasitic loss (W)	Total loss
Medium	12	20K	1.00	1.093	12.95	12.95
High	6	20K	1.43	1.01	11.61	11.61
Total	18	---	2.44	2.09	20.02	24.56

Fig. 14. Phase current in proposed DTC

Fig. 15. Phase voltage showing 5 level in proposed DTC

Fig. 16. Output torque in conventional DTC (1V=1Nm)

Fig. 17. Output torque in proposed DTC (1V=1Nm)

Fig. 18. Experimental setup.

Where P_{cond} represent conduction loss, $I_{on(rms)}$ is the drain current when the MOSFET is on and $R_{ds,on}$ is the on state drain to source resistance.

$$P_T = \frac{V_{off} I_{on} f_s}{2} (t_{s,on} + t_{s,off}) \quad (12.b)$$

Where P_T represent the transition loss (on time and off time) V_{off} is off state drain source voltage, $t_{s,on}$ and $t_{s,off}$ are the transition time. f_s is the switching frequency.

$$P_{pc} = C_{oss} V_{off}^2 I_{on} f_s \quad (12.c)$$

Where, P_{pc} stand for loss due to charging/discharging of the drain-source parasitic capacitor and C_{oss} is the output capacitance of the MOSFET

Table 4. Comparison among existing MLI based DTC and proposed DTC

Existing DTC	Reference	Proposed DTC drive
-Topology: Cascaded H-bridge -Controller: Switching table based DTC -Hardware validation: Not included -Number of switch: 24 -Switching loss analysis: Not included -Vector selection strategy: Not clearly mentioned. It has been presented in tabular form. There is no clear indication of how the vectors are selected.	[32]	-Topology: Cascaded hybrid bridge -Controller: Optimized ST-DTC -Hardware validation: Included -Number of switch: 18 -Switching loss analysis: Included -Vector selection strategy: Graphically presented how the vectors have been selected based on the control command.
-Topology: Cascaded H-bridge -Controller: SVM-DTC -Hardware validation: Not included -Number of switch: 24 -Switching loss analysis: Not included	[25]	-Topology: Cascaded hybrid bridge -Controller: Optimized ST-DTC -Hardware validation: Included -Number of switch: 18 -Switching loss analysis: Included
-Topology: Cascaded H-bridge -Controller: PSSVM-DTC -Hardware validation: Not included -Number of switch: 36 -Switching loss analysis: Not included -THD analysis: Not included	[33]	-Topology: Cascaded hybrid bridge -Controller: Optimized ST-DTC -Hardware validation: Included -Number of switch: 18 -Switching loss analysis: Included -THD analysis: Included
-Topology: Cascaded Symmetrical and Asymmetrical H-bridge -Controller: Switching table based DTC -Number of switch: 24 -Switching loss analysis: Not included -Content: The title of the paper does not clearly agree with the content. Specifically, there is no comparison of Symmetrical and Asymmetrical H-bridge based ST-DTC in terms of Simulation and hardware validation.	[34]	-Topology: Cascaded hybrid bridge -Controller: Optimized ST-DTC -Number of switch: 18 -Switching loss analysis: Included -Content: Content of the paper agreed with the title.

The comparison among the proposed MLI based DTC and similar existing type DTC is listed in Table 4. This comparison shows that proposed topology reduces the number of switches. Consequently, in terms of topology the proposed topology is efficient and reliable. It can also be visualized that DTC with higher number of voltage level, irrespective to control technique applied, is somewhat limited to simulation. As a result, it is hard to get any quantitative comparison of experimental result among them. Switching table based control is simple compared to SVM technique, even though its complexity increases greatly when the number of vectors is increases. Therefore, it is difficult to distribute the vectors for different control demands. However, once the switching table is designed, the overall implementation of the controller becomes easier.

In summary, switching table based DTC with multilevel inverter introduced in this paper can be used efficiently as induction motor drive and worthy to introduce as industrial grade variable speed drive.

8. Conclusion

Due to several advantage of DTC over FOC and other algorithm for induction motor drive, research and improvement of convention DTC is necessary. In this paper a DTC scheme utilizing five levels cascaded hybrid H-bridge MLI is proposed as an improvement of its ancestor. Thanks to 61 suitable voltage vector combination inherently generated by five level MLI which facilitate the control strategy of proposed DTC scheme. Conception of basic DTC scheme is modified and extended for five levels inverter. Multilevel torque and flux hysteresis controller is designed by simply

dividing the Clarke plane into twelve equal sectors. Sector selection has been done by empirical equation. Simulation based study revealed that the steady state performance of the IM is improved noticeably. These performances have been experimentally validated and found close similarity between simulation and hardware result.

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