Evaluation of Radio-Frequency Performance of Gate-All-Around Ge/GaAs Heterojunction Tunneling Field-Effect Transistor with Hetero-Gate-Dielectric by Mixed-Mode Simulation

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Abstract – In this work, the frequency response of gate-all-around (GAA) Ge/GaAs heterojunction tunneling field-effect transistor (TFET) with hetero-gate-dielectric (HGD) and pnpn channel doping profile has been analysed by technology computer-aided design (TCAD) device-circuit mixed-mode simulations, with comparison studies among ppn, pnpn, and HGD pnpn TFET devices. By recursive tracing of voltage transfer curves (VTCs) of a common-source (CS) amplifier based on the HGD pnpn TFET, the operation point (Q -point) was obtained at $V_{DS} = 1$ V, where the maximum available output swing was acquired without waveform distortion. The slope of VTC of the amplifier was 9.21 V/V (19.4 dB), which mainly resulted from the ponderable direct-current (DC) characteristics of HGD pnpn TFET. Along with the DC performances, frequency response with a small-signal voltage of 10 mV has been closely investigated in terms of voltage gain (A_v), unit-gain frequency (f_{unity}), and cut-off frequency (f_T). The Ge/GaAs HGD pnpn TFET demonstrated $A_v = 19.4$ dB, $f_{unity} = 10$ THz, $f_T = 0.487$ THz and $f_{max} = 18$ THz.

Keywords: Frequency response, Gate-all-around, Heterojunction, Tunneling field-effect transistor, Hetero-gate-dielectric, TCAD, Mixed-mode simulation

1. Introduction

Conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) driven by drift and diffusion have a lower limit in subthreshold swing (S) (~ 60 mV/dec) at room temperature due to thermionic emission. The irreducible S is a hindrance in enhancing the on-state current (I_{on}) while maintaining a sufficiently low off-state current (I_{off}), which is also closely related with operation voltage scaling. For this reason, there have been efforts to reduce S below 60 mV/dec for improved switching characteristics [1-4]. Tunneling field-effect transistors (TFETs) operated by band-to-band (BTB) tunneling have been widely researched for its plausible feature of small S dropping below the theoretical limit of MOSFETs [5-10]. Also, TFETs have stronger immunity against short-channel effects (SCEs) owing to its tunneling-based operating principle and channel doping profile different from those of conventional MOSFETs [11]. Low on-state current (I_{on}) has been pointed out as a drawback of silicon (Si) TFET and efforts have been made to enhance the current drivability of many aspects which include trials of

applying particular structures [12-14] and low bandgap materials [15]. Besides, it can be achieved by using compound materials to obtain low effective mass and small bandgap [16, 17]. Several device geometry have been researched in order to diminish ambipolar current and an encumbering effect of gate electric field [18-21]. In this work, a TFET device operating by approaches to achieve higher I_{on} of which validation have been confirmed in terms of high-frequency characteristics, especially frequency response. The device is equipped with both hetero-gate-dielectric (HGD) materials and n-type insertion layer boosting the BTB tunneling [12, 13]. Furthermore, the device channel consists of Ge (source) and III-V compound semiconductor (channel and drain) for enhancing the tunneling efficiency (higher I_{on}) at the source side and suppressing I_{off} at the drain side. Besides the betterments in current characteristics, Ge/(Al)GaAs heterojunction has a good interface owing to its little lattice mismatch [16, 17]. Considering approaching more practical and accurate situation, we are focused on tunneling current via nonlocal trap in the relatively wide tunneling width region of the previous researches [22]. In terms of circuit operation, it is expected that the device with HGD and with n-type insertion layer has the immunity to trap-assisted tunneling (TAT) mechanism and decent high-frequency characteristics even if it is set to lower input Q bias. The channel had a gate-all-around (GAA) structure for enhancing the gate controllability

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in mainly focused and its characteristics are compared with those of devices with ppn and pnpn channels. The frequency responses are investigated from common-source (CS) amplifier embedding the Ge/GaAs HGD pnpn TFET, one of the most fundamental functional block in the analog circuit, by mixed-mode simulation to obtain more accurate solutions through monitoring the real-time interactions between the device and circumference circuit components [23].

2. Device Schemes and Direct-Current (DC) Performances

Fig. 1 shows the cross-sectional view of nanowire Ge/GaAs heterojunction TFET with (a) ppn channel, (b) pnpn channel, and (c) hetero-gate-dielectric (HGD) and n-insertion layer (pnpn channel).

These devices will be shortly called ppn, pnpn, and HGD pnpn TFETs, respectively. In device simulation, the doping concentrations were p^+ Ge source of 10^{20} cm^{-3} , p GaAs channel of 10^{16} cm^{-3} , and n^+ GaAs drain of 10^{18} cm^{-3} , and GaAs n-type insertion layer of 10^{18} cm^{-3} . For comparison with HGD pnpn device regarding circuit level performance, ppn and pnpn device are made like reference device [13, 22]. Multiple models were employed for higher accuracy in simulation results, including concentration-dependent mobility model, Shockley-Read-Hall recombination model, bandgap narrowing model, and BTB model by Hurkx assisted by non-local BTB tunneling calculation, quantum model, and trap-assisted

tunnel (TAT) model. The device is designed to have channel length (L_{ch}) of 30 nm, channel radius (r_{ch}) of 10 nm, and gate dielectric thickness (T_{ox}) of 2 nm. The lengths of n-insertion layer ($L_{\text{ch-n-GaAs}}$) and HGD (L_{HG}) were adjusted for obtaining fully depleted tunneling junction and both of them were 8 nm. HGD consisted of hafnium oxide (HfO_2) (source side) with a relativity permittivity (ϵ_r) of 25 and aluminum oxide (Al_2O_3) (drain side) with $\epsilon_r=9.3$. Copper (workfunction (ϕ_m) = 4.4 eV) was used for the gate metal. From a fabrication point of view, Ge and GaAs can be epitaxially grown by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) forming good interfacial status owing to genuinely little lattice mismatch [24]. Combinational uses of plasma laser annealing doping (PLAD), excimer laser annealing (ELA), and dopant profile-steepening implantation (DPSI) can be considered as the most recent possible techniques to obtain high doping concentration with nearly abrupt junctions [25-27]. Fig. 1(d) shows schematic of CS amplifier embedding a TFET. Signal resistance (R_{sig}) and drain resistance (R_D) were selected to be 50 Ω and 4 k Ω , respectively, by recursive simulations to obtain symmetric output swing [22].

Fig. 2(a) shows the transfer characteristics (I_D - V_{GS}) of

Fig. 1. Schematics of simulated devices and circuit. Cross-sectional view of (a) ppn, (b) pnpn, and (c) HGD pnpn TFETs. (d) Configuration of CS amplifier with the TFETs.

Fig. 2. (a) Transfer characteristics (I_D - V_{GS}) of PPN structure, PNPn structure, and HGD PNPn structure with and without TAT. (b) Transconductance of PPN structure, PNPn structure, and HGD PNPn structure with TAT.

the simulated devices with and without TAT model for pnpn, pnpn, and HGD pnpn TFETs. When gate voltage (V_{GS}) is low, TAT is dominant over BTB tunneling due to thick tunneling barrier between source and channel, which is proven by the fact that the I_{off} makes a difference near $V_{GS} = 0$ V depending on whether TAT model is turned on or not. As V_{GS} increases, the effect of TAT is weakened and BTB tunneling begins to dominate. Tunneling probability, $T(E)$, induced by Wentzel-Kramers-Brillouin (WKB) approximation is expressed as

$$T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar\xi}\right) \quad (1)$$

where m^* is the reduced effective mass in the average sense of electron (m_e^*) and hole (m_h^*) effective masses, E_g is bandgap energy, e is electron charge, ξ is the electric field, and $\hbar$ is the reduced Planck's constant [28, 29]. Aided by the equation for Hurkx's BTB tunneling model, S for TFET can be formulated in a closed form as below.

$$S = \frac{V_{GS}^2}{5.75(V_{GS} + \text{constant})} [mV/dec] \quad (2)$$

where constant in the denominator is determined by device dimensions and material properties [30]. Higher V_{GS}

increases S from Eq. (2), by which it is expected that TFET is suitable to low-power operation for steeper switching slope. S of the devices in Figs. 1(a)-(c) are extracted to be 31.5 mV/dec, 22.4 mV/dec, and 22.3 mV/dec, respectively, as shown in Fig. 2(a). Slopes much steeper than 60 mV/dec are obtained and further improvements are made in the devices with pnpn and HGD pnpn structures. Transconductances (g_m 's) of the devices are depicted in Fig. 2(b), which shows prominent enhancement as the device is evolved to have from pnpn to pnpn and HGD pnpn structures.

Figs. 3(a) and (b) show the output characteristics (I_D - V_{DS}) of the designed devices with and without TAT models at different gate voltages, $V_{GS}=0.6$ V and 1.0 V, respectively. Superlinear behaviors of I_D in the low V_{DS} region are observed as reported in a previous literature [31]. In both cases, I_D of pnpn TFET is increased by an amount of 15% of its initial value by activating the TAT model in the simulation compared with the current obtained without the model, while pnpn and HGD pnpn devices demonstrate negligibly small change. Increment in I_D of pnpn TFET is originating from a fact that its tunneling barrier is not thin enough to suppress the TAT current and substantially retards the BTB tunneling as described in Figs. 4(a) and (b). On the other hand, pnpn and HGD pnpn TFETs are immune to TAT so that BTB tunneling is more readily dominant in the operations [32], of which merit comes with circuit performances clearly as will be shown in a later section.

Fig. 3. (a) I_D - V_{DS} of TFETs with and without TAT at $V_{GS} = 0.6$ V, (b) at $V_{GS} = 1.0$ V.

Fig. 4. Energy band diagrams of depletion layer of each device at (a) $V_{GS} = 0.6$ V, (b) $V_{GS} = 1.0$ V.

Table 1. Summary of specific device performances.

	PPN	PNPN	HGD PNPN
I_{on} (A/ μ m)	5.34e-4	1.36 e-3	2.95e-3
I_{off} (A/ μ m)	1.40e-16	8.70e-17	5.81e-16
on/off ratio	3.81e12	1.56e13	5.08e12
V_T (V)	0.40	0.30	0.27
S (mA/decade)	31.5	22.4	22.3

Specific device performances such as on-state current, off-state current, on / off ratio, threshold voltage and subthreshold swing are summarized in Table 1.

3. Circuit Performances

Fig. 5(a) depicts voltage transfer characteristics (VTCs) of a CS amplifier using Ge/GaAs heterojunction TFET. The circuit simulations have been also carried out with and without TAT model to study in comparison its effect on circuit performances. First of all, the operating point (Q -point) needs to be positioned in order to have maximum slope on the VTC curve at Q -point, which leads to the maximum amplification. Input bias was varied with device types for obtaining the optimum condition, which were $V_{IN} = 1.16$ V for ppn TFET, $V_{IN} = 0.78$ V for npn TFET, and $V_{IN} = 0.62$ for HGD npn TFET. Along with output voltage (V_{OUT}) of the Ge/GaAs TFET-embedded CS amplifier, the slope of VTC curve (dV_{OUT}/dV_{IN}) is plotted as a function of V_{IN} as shown in Figs. 5(b)-(d). The maximum dV_{OUT}/dV_{IN} values were -6.66 V/V for ppn TFET, -7.82 V/V for npn TFET, and -11.28 V/V for HGD npn TFET. The DC performance of CS amplifier as an inverter is also improved as the main transistor is evolved from ppn TFET to npn and HGD npn TFETs. The next important step in biasing an amplifier should be to check if there is no distortion in output swing. Although it was verified that the amplitude of small-signal voltage ($|v_{in}| = 10$ mV) was not large enough to make any distortion in output swing at the selected Q -point above, the output bias for Q -point was further adjusted to $V_{DS} = 1$ V so that wide enough output window as well as symmetry in maximum swing could be more stably secured [22]. For this goal, drain resistance can be precisely controlled in through recursive analyses of load-line at the Q -point. Considering the conditions for BTB tunneling, input voltages of the CS amplifiers with ppn, npn, and HGD npn TFETs were set to 0.59 V, 0.74 V, and 1.15 V, respectively. The CS amplifier with ppn TFET shows V_{IN} shift as depicted in Fig. 5(b), which is mainly due to the increase of I_D caused by TAT as previously mentioned in Fig. 3(a). Considering the effect of TAT, the input bias was set to $V_{IN} = 1.11$ V for the CS amplifier with ppn TFET. After further adjusting of the bias conditions, the derivatives of VTC at the Q -points (dV_{OUT}/dV_{IN}) as the most crucial factor in small-signal amplification, have been slightly changed to -5.3 V/V

Fig. 5. Voltage transfer characteristics (VTCs) of (a) TFETs; (b) PPN TFET with and without TAT; (c) PNPN TFET with and without TAT, and (d) HGD PNPN TFET with and without TAT.

(14.5 dB), -6.6 V/V (16.4 dB), and -9.21 V/V (19.4 dB) for the CS amplifiers with ppn, npn, and HGD npn TFETs, respectively. The prominently high g_m (as was confirmed

by Fig. 2(b)) of HGD npn TFET plays a major role in enhancing the amplification ratio.

Figs. 6(a) and (b) demonstrate the frequency responses of the CS amplifiers with ppn, npn, and HGD npn TFETs regarding voltage gain (A_v) and phase change, respectively. The results were obtained by device-circuit mixed-mode simulations at the final Q -points. The A_v values in decibel (dB) correspond to the maximum slopes on the VTC curves (amplification ratios) obtained in the optimization processes travelled above. In Fig. 6(a), the unity gain frequencies (f_{unity}) (intercept crossing 0 dB) of the CS amplifiers with ppn, npn, and HGD npn TFETs, are 8 THz, 9.5 THz, and 10 THz, respectively. This figure of merit (FoM) is one of the crucial in factors in the analog circuits, which implies that circuits embedding the TFETs in this work would have a wide range of operating frequency and its importance is more revealed as the system employs a negative feedback [33]. Fig. 6(b) shows phase shifts of -270° , of which system can be mathematically described by a transfer function with two right-half-plane (RHP) poles and one left-half-plane (LHP) zero [22]. The little curvatures infer that the poles and zero are closely located in the s -plane.

In Fig. 7, current gain and unilateral power gain of the circuits have been extracted. The cut-off frequency (f_T), which is defined as the frequency interception with the unity current gain (0dB), is generally specified as

(a)

(b)

Fig. 6. (a) Magnitude response of TFETs; (b) Phase shift response of TFETs.

Fig. 7. Current gains and unilateral power gains of each PPN, PNP, and HGD PNP TFET.

Table 2. Capacitances and transconductances of each PPN, PNP and HGD PNP TFET at each input bias.

	PPN	PNP	HGD PNP
C_{gs} (aF)	12.6	10.8	10.8
C_{gd} (aF)	4.60	3.45	3.46
C_{gg} (aF)	17.2	14.2	14.2
g_m ($\mu A/V$)	182	67.6	43.6

$$f_T = \frac{g_m}{2\pi C_{gg}}$$

where C_{gg} is sum of gate-source capacitance and gate-drain capacitance [34]. Table 2 shows capacitances and transconductances extracted by radio-frequency gate-all-around TFETs modeling in the different Q -points [35]. These capacitances of each device are extracted for further analyzing into high frequency response. The extracted f_T of PPN, PNP, and HGD PNP TFET are revealed as 1.68THz, 0.76THz, and 0.487THz, respectively. The PPN and PNP device, which have relatively high input biases, can have high gate-source capacitances and high transconductances. While HGD PNP device has low input bias, HGD device has high gate-source capacitance due to high- k hetero-gate-dielectric near the source. For this reason, f_T of HGD npn device is lower than ppn device.

On the other hand, Unilateral power gain (U_{max}), which is the measurement of the quality of active devices over the entire frequency range of interest, can be extracted as

$$U(f) = \frac{|Y_{21} - Y_{12}|^2}{4\{\text{Re}(Y_{22})\text{Re}(Y_{11}) - \text{Re}(Y_{21})\text{Re}(Y_{12})\}}$$

where Y s are linear two port network parameter [36]. The maximum oscillation frequency (f_{max}), which are crossing 0dB of U_{max} in Fig. 7, are 9THz, 16THz, and 18THz, respectively.

This result reveals that low-power operation is made possible by adopting the HGD npn TFETs in high-frequency circuit applications.

4. Conclusion

In this work, high-frequency characteristics of GAA Ge/GaAs heterojunction HGD pnpn TFET have been analyzed with a particular interest in frequency responses, by device-circuit mixed-mode simulations. The study has been carried out in comparison with devices with pnp and pnpn (but without HGD) channel doping profiles for more stringently verifying the superiority of the pnpn HGD device. Higher current drivability and transconductance and immunity to TAT mechanism were obtained from the pnpn HGD TFET and a common-source amplifier with the device was schemed for having a closer look into the contributions of the device in circuit applications. Voltage characteristics of devices are discussed with details in steps determining the circuit Q -points. At the optimum operating condition, the amplifier demonstrated $A_v=19.4$ dB, f_{unity} (frequency at unity A_v) =10THz, and $f_T=0.487$ THz, and $f_{\text{max}}=18$ THz GAA Ge/GaAs heterojunction HGD pnpn TFET has a number of advantageous features for driving transistor in advanced integrated circuits for low-power high-frequency applications.

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