Digital Control of Secondary Active Clamp Phase-Shifted Full-Bridge Converters
Yanbo Che†, Yage Ma*, Shaoyun Ge*, and Dong Zhu*

†*Key Laboratory of Smart Grid of Ministry of Education, Tianjin University, Tianjin, China

Abstract

A DSP-based self-adaptive proportional-integral (PI) controller to control a DC-DC converter is proposed in this paper. The full-bridge topology is adopted here to obtain higher power output capability and higher conversion efficiency. The converter adopts the zero-voltage-switching (ZVS) technique to reduce the conduction losses. A parallel secondary active clamp circuit is added to deal with the voltage overshoot and ringing effect on the transformer’s secondary side. A self-adaptive PI controller is proposed to replace the traditional PI controller. Moreover, the designed converter adopts the constant-current and constant-voltage (CC-CV) output control strategy. The secondary active clamp mechanism is discussed in detail. The effectiveness of the proposed converter was experimentally verified by an IGBT-based 10kW prototype.

Key words: Digital control, Phase-shifted full-bridge, Secondary active clamp, Self-adaptive PI control

I. INTRODUCTION

Nowadays, clean and renewable energies including fuel cells, wind energy, photovoltaic, etc., have been widely applied to achieve environmentally-friendly objectives. Converters play key roles in the energy transformation [1].

As is known, a full-bridge converter can possess a higher power density by increasing the carrier frequency of the power transistors. However, the energy conversion efficiency is reduced due to the switching loss of the higher switching frequency, worsening the thermal and electromagnetic interference effects. In order to solve these problems, a phase-shift full-bridge (PSFB) converter with ZVS is proposed here. Some of the prominent features of this topology include high efficiency, high power density, and ZVS that is easy to achieve [2]. ZVS for all of the switches can be obtained by utilizing the transformer’s leakage inductance and the intrinsic capacitance of the switches without any additional circuitry [3,4]. In high power level applications, for example higher than 5 kW, insulated gate bipolar transistor (IGBT) devices are usually preferred and predominantly used as power switches [5,6].

DC-DC converters usually utilize rectifiers at the output side. However, rectifiers having a relatively long recovery time will produce voltage spikes. The parasitic capacitance of the rectifiers will resonate with the transformer’s leakage inductance causing high frequency oscillations on the transformer’s secondary side [3].

There have been some attempts to overcome the aforementioned drawbacks. A resistance-capacitor-diode snubber circuit was proposed and it works well by limiting the peak value of the rectifier voltage oscillation [7, 8]. However, a power loss in the snubber resistance degrades the system efficiency when the output power increases.

The converter proposed in [2] employs an asymmetric auxiliary circuit to provide reactive current for the full-bridge semiconductor switches, which guarantees ZVS at the turn-on time. Although this control scheme is able to determine the optimum value of the reactive current injected by the auxiliary circuit, extra conduction losses in the power MOSFETs as well as in the auxiliary circuit can not be eliminated.

Papers [9] and [10] add auxiliary passive networks into the traditional converter and all of the primary switches can achieve ZVS in the entire load range. Furthermore, the parasitic oscillations of the rectifier voltage are lower because the leakage inductance can be designed to be rather small. However, it is a passive method not a fundamental solution for the oscillation between the leakage inductance and the
parasitic capacitance of the rectifier.

In addition, there have been some improvements in the control strategy of the converter. The converter in paper [11] adopts a constant-current and constant-voltage (CC-CV) charging strategy to charge lithium-ion battery packs. To improve the transient of the voltage regulation during load variations, a Probabilistic Fuzzy Neural Network (PFNN) controller is proposed to replace the traditional PI controller and to have the ability of online learning algorithms.

A novel ZVS PSFB PWM converter is proposed here. In order to reduce the voltage oscillations and the duty cycle loss on the transformer’s secondary-side, a secondary active clamp circuit is added in this topology. The active clamp circuit consists of an IGBT, a capacitor and a diode. The voltage stress of the switches on the primary side is reduced and the ringing effect of the rectifier switches is restrained [12]. The PSFB converter realizes ZVS for the leading legs over a wide load range. The converter uses a digital signal processor (DSP) as the control core. The digital control core adopts a self adaptive PI control strategy, which provides good control performance even in harsh conditions and is simple when compared to that in paper [11]. In addition, the implementation of AD sampling and fault protection are also incorporated into the DSP [13], [14]. Experimental results are presented to verify the validity and strong points of the proposed converter.

II. OPERATION ANALYSIS OF THE CONVERTER AND ITS DIGITAL FULFILLMENT

The main topology of a PSFB converter with a secondary active clamp circuit is shown in Fig. 1. There is a DC blocking capacitor $C_{ab}$ in the transformer’s primary side that is not sketched here. The converter is constructed using a full-bridge converter, a high frequency transformer $T_1$, and a LC low-pass filter. Switches $Q_1$-$Q_4$ are the working switches in the full bridge. Diodes $D_1$-$D_4$ serve as a rectifier. The output power is controlled by adjusting the phase-shift angle $\phi$. In the steady state, the relationship between the input voltage $V_{in}$ and the output voltage $V_o$ can be represented by the following equation:

$$V_o = n_o \frac{\Phi}{\pi} V_{in}$$  \hspace{1cm} (1)

Where $n_o = N_o/N_p$ is the transformer turns ratio, $N_p$ is the transformer primary turns, and $N_o$ is the transformer secondary turns.

A. Phase-Shift Full-Bridge Operation Analyses

One working cycle of the PSFB converter can be divided into 12 operation modes ($t_0$-$t_{12}$). It is enough to analyze the first 6 operation modes since the following (7-12) modes are similar to the preceding 6 modes. The corresponding theoretical waveforms are depicted in Fig.2.

1) Mode 1 ($t_0$-$t_1$): During this period, the IGBTs $Q_1$ and $Q_4$ are conducted. The transformer’s primary voltage $V_{ab}$ is equal to the input voltage $V_{in}$. The slope of $I_p$ is depicted as:

$$\frac{di_p}{dt} = \frac{V_{ab} - (V_o / n_o)}{L_i + (L_n / n_o^2)}$$  \hspace{1cm} (2)

2) Mode 2 ($t_1$-$t_2$): $S_1$ turns off at $t_1$ and the current $I_p$ flows through $C_{ab}$ (the parallel buffer capacitor of $Q_4$). $C_{ab}$ discharges when $V_{ab}$ gradually decreases. Both sides of the transformer are still coupled. The secondary inductor is large. Therefore, $I_p$ remains unchanged. This mode is usually known as the leading arm transition.

3) Mode 3 ($t_2$-$t_3$): The intrinsic diode $D_{ab}$ ($Q_2$’s reverse parallel diode) forward conducts and serves as a channel for $I_p$ to flow through. During this period $Q_2$ can turn on under zero-voltage. The current $I_p$ is predicted as:

$$\frac{di_p}{dt} = -\frac{V_o / n_o}{L_i + (L_n / n_o^2)}$$  \hspace{1cm} (3)
4) Mode 4 (t3-t4): Q1 turns off under zero-voltage at t0. The primary current $I_p$ charges capacitor $C_{s}$ while capacitor $C_p$ gets discharged. The voltage $V_{rec}$ gradually decreases and drops to $-V_o$ at t4. This negative voltage forces the secondary diodes $D_2$ and $D_4$ to conduct. $D_2$ and $D_4$ can not be shut down immediately and eventually make the transformer’s secondary short-circuited. Thus, the transformer becomes decoupled. This mode is also known as the lagging arm transition.

5) Mode 5 (t4-t5): $D_3$ forward conducts at t4 and serves as a channel for $I_p$. $Q_3$ can turn on under zero-voltage during this period. The current $I_p$ is predicted as:

$$\frac{dI_p}{dt} = \frac{V_o}{L_{o}}$$

(4)

6) Mode 6 (t5-t6): The primary current $I_p$ drops to zero at t5 and it flows through $S_2$ and $S_3$. $I_p$ begins to grow reversely and its pace is the same as in the preceding mode. $I_{rec}$ also gradually increases and is equal to $I_p$ at t6. $D_1$ and $D_2$ turn off and both windings of the transformer regain their coupling.

B. Ringing Effect and the Secondary Active Clamp Circuit Operation Analysis

The transformer’s secondary side in a typical PSFB converter is depicted in Fig. 3. The rectifier diodes have a relatively long reverse recovery time and will cause voltage spikes when it is reversely cut-off. The voltage $V_{rec}$ on the rectifier can be seen as a step voltage. Under the action of $V_{rec}$, the parasitic capacitor of the rectifier diodes $C_p$ will resonate with the leakage inductance $L_{k}$, thus causing high frequency oscillations on the secondary side. This phenomenon is called the ringing effect [15], [16].

The oscillation frequency:

$$f_{ring} = \frac{1}{2\pi} \frac{L_{o}}{C_p n_{o}^2}$$

(5)

The defects of the voltage spike include electric stress on the components, producing EMI noise and affecting the inverter’s output characteristic. There are four commonly used measures to restrain peak oscillations [17], [18]:

1) Connecting the RC absorbing circuit and rectifier diodes in parallel. This method is easy to realize. However, it has greater losses in superpower circuits and does not perform well.

2) Adding a clamp diode at the primary side can restrain oscillations on the secondary to some extent. However, it cannot completely eliminate oscillations.

3) Connecting a saturated inductance in series with the rectifier circuits to restrain the transient change when low current flows through. This is an easy method. However, its main drawback is the heat trouble generated by the saturated inductance.

4) Adding an active clamp circuit in parallel with the rectifier output side can efficaciously suppress peak oscillations and release the energy to the loads. This method needs additional control circuits.

An active clamp circuit is adopted here to reduce the voltage spike and ringing effect. The clamp capacitance $C_i$ is used to resonate with the leakage inductance $L_{k}$. $C_i$ absorbs voltage in the first half of the switching cycle and releases the energy to the load in the second half. The clamp capacitance $C_i$ keeps its voltage unchanged in a cycle and its average charging and discharging current sums up to zero. The whole switching cycle can be seen in Fig. 4. It is advised to choose a clamp capacitance that is much larger than $L_{k}$ so that the resonant period is relatively long, as well as the charging and discharging current can be restrained.

The working cycle of $Q_i$ (the secondary active clamp’s switch) is divided into 4 operation modes. The modes are analyzed as follows.

1) Mode 1 ($t_0-t_1$) is shown in Fig. 5(a). The voltage $V_{rec}$ is established at $t_0$. At the same time $Q_i$ turns off. The leakage inductance of the transformer and the parasitic capacitor of the diode resonates with the clamp capacitor.
are represented by equation (7).

represented by two dependent sources.

is shown in Fig. 5. Operation modes of the clamp circuit.

is the duty cycle perturbation.

A. Small Signal Circuit Model of a PSFB DC-DC Converter

The small-signal analysis of a PSFB converter has been carefully studied in paper [11] and paper [19]. The effective duty cycle of the transformer secondary voltage is:

$$d_{eff} = D_{eff} + \hat{d}_{eff}$$

Where $D_{eff}$ is the duty of the operating point and $\hat{d}_{eff}$ is the duty cycle perturbation. $d_{eff}$ depends on the duty cycle $d$ of the primary voltage as well as the filter inductor current $i_{Ls}$, the leakage inductance $L_{s}$, the input voltage $V_{dc}$, and the switching frequency $f_{s}$. Thus, the small-signal transfer function of this converter depends on $L_{s}$, $f_{s}$, and the perturbations of the filter inductor current, $i_{Ls}$, the dc-link voltage $\hat{V}_{dc}$ and the duty cycle of the primary voltage $\hat{d}$. The open-loop transfer function is obtained as:

$$G_{oa} = \frac{\hat{V}_{dc}(s)}{d(s)} = \frac{n_{s}V_{dc}}{s^{2}L_{s}C_{r} + s((L_{s}/R_{load}) + (R_{d}/R_{load}) + 1}$$

Where $\hat{V}_{dc}$ is the perturbation of the output voltage. The parameters in this transfer function are listed as follows: $V_{dc}=650V$, $L_{s}=284uH$, $C_{r}=75uF$, $m_{o}=11/13$, $R_{load}=30\Omega$, $f_{s}=20kHz$, $L_{s}=10uH$, and $R_{d}=0.573 \Omega$. The designed PSFB converter has a phase margin of $1^{\circ}$ and a bandwidth of 1847 Hz.

B. Self-Adaptive PI Controller Design

It is well known that switching DC-DC converters with parameter uncertainties and variable operating conditions are highly nonlinear systems. As a result, the conventional control method based on the averaging and linearization techniques will not provide good dynamic performance and can even make the system unstable [20], [21].

A self-adaptive PI control strategy is proposed here. The converter can work in either CC output mode or CV output mode as shown in Fig. 7 (a). When it is in CV mode, to make the output voltage quickly track the command voltage, the proportional factor $K_{p}$ needs to vary in accordance with the actual output voltage. The proportional factor is defined as:

$$K_{p} = \frac{\Delta V}{\Delta V}$$

Where $\Delta V$ is the difference between the expected output voltage $V_{e}$ and the actual output voltage $V_{o}$. $D$ is defined as:

$$D = \frac{V_{e}}{V_{o}}$$

The integral factor $K_{i}$ is then defined as:

$$K_{i} = \frac{K_{p}}{k}$$

Where $k$ is an empirical coefficient and ranges from 3 to
The leading arm and the lagging arm. The output voltage is 

\[ v_o(s) = G_{vd}(s) \cdot d_1(s) \]

Sampling value conversion interrupt service function handles 
generation of the main loop are included in the main program. The main loop ISRs, are depicted in Fig. 8(b).

C. DSP Based Controller Design

A TMS320F2812 DSP is adopted here to serve as the control core of the system. The control block consists of two self-adaptive PI controllers, two limiters and a PWM generator. \( v_o \) is the output voltage command; \( v_o \) is the output voltage; \( i_o \) is the output current command; \( i_o \) is the output current; and \( U^* \) is the limited value form the limiter. Whether the PWM generator works in CC mode or CV mode is selected by the user at startup.

For voltage control, the PI voltage controller \( G_v(s) \) is shown in Fig. 7(b). Where \( v^*(s) \) is the perturbation of the output voltage command, \( \hat{v}_o(s) \) is the perturbation of the output voltage, and \( \hat{d}_1(s) \) is the perturbation of the duty cycle for the transformer’s primary side. The open loop transfer function \( T_v(s) \) can be derived from Fig. 7(b):

\[ T_v(s) = G_v(s) \cdot G_d(s) \] (12)

The same way can be used to analyze the current PI control loop and the transfer function \( T_i(s) \) can be derived from Fig. 7(c):

\[ T_i(s) = G_i(s) \cdot G_d(s) / R_{load} \] (13)

For the required phase margin and bandwidth of the transfer function \( T_v(s) \) and \( T_i(s) \), the compensators \( G_v(s) \) and \( G_i(s) \) should be carefully designed.

The DSP hardware resources are distributed as shown in Fig. 8(a). The flow charts of the main program and the two ISRs, are depicted in Fig. 8(b). The parameters and I/O initialization, the peripheral and interrupt settings and the main loop are included in the main program. The main loop deals with the procedure of self-adaptive PI control, PWM generation and the other controls in the converter. The AD interrupt service function handles the interrupt response and sampling value conversions. The AD sampling is triggered in the 25us interrupt service function, and the average values are calculated every 20 times. Then these average values are used in the self-adaptive PI controller to produce the phase shift angle for the PWM generator.

D. Digitally Fulfilled Phase-Shifted Control

The duty ratios of the four switches’ driving signals are 50%. The driving signals on the same arm are complementary, having a 180 degree phase lag. There is a phase lag between the leading arm and the lagging arm. The output voltage is 

\[ v_o(s) = \sum e_i(s) \]

\[ i_o(s) \]

regulated by adjusting this phase. This is the so-called phase-shifted control technique [22]-[24].

A TMS320F2812 DSP controller owns two event manager modules (EVA and EVB). \( T_i \) from EVA and \( T_{r} \) from EVB are applied to generate PWM for the leading and lagging arms, respectively. \( T_iPR \) is used to configure the switching period, \( T_iCMP \) determines the duty ratio, while \( T_iCNT \) denotes the counter register values and is used to configure the phase-shifted angle.

The implementation steps include the following:

1) Configure the \( T_iPR \) and \( T_iCMP \) registers to generate two sets of PWM waves. The two PWM waves share the same switching frequency and both have a 50% duty ratio. PWM1/PWM2 are for the leading arms and PWM7/PWM8 are for the lagging arms.

2) Let the phase-shifted angle be \( \alpha \). Set \( T_iCNT = 0 \) and \( T_iCMP = T_iPR \cdot \alpha / 360^\circ \) so that PWM7 lags PWM1 \( \alpha \) degrees and PWM8 lags PWM2 \( \alpha \) degrees.

E. Digital Realization of the Secondary Active Clamp

\( T_2 \) from the EVA module is used to create the PWM waveform for the clamp switch \( Q_2 \).

The details are represented as follows:
The criterion for ZVS is that enough energy to charge and discharge the paralleling capacitance in the IGBT. The achievement of ZVS in leading leg is not as easy as that in the lagging leg. The transformer’s primary side and secondary side are coupled in the switching process as analyzed in mode 2. The inductance L1 and L2 are connected in series and the current I2 remains approximately unchanged. The criterion for the lagging leg’s ZVS is:

\[
E = \frac{1}{2} L_2 I_2^2 > \frac{1}{2} C_l V_2^2 + \frac{1}{2} C_T V_2^2 \]

\[
t_{d(\text{lag})} > 2 C_{\text{load}} V_2 / I \]  

where \( t_{d(\text{lag})} \) is the dead time between \( Q_1 \) and \( Q_2 \). The transformer’s primary side and secondary side
determined that current charging current as shown in Fig.4. When \( t \) before the duty cycle loss on transformer increase. Otherwise should synchronize with the rectifier’ voltage overshot. Usually equation (15) is easy to satisfy but the lagging leg’s ZVS realization needs carefully design.

B. Loss of Duty Cycle

The duty cycle on the transformer’s secondary side \( (D_s) \) is smaller than that on the primary side \( (D_p) \). In addition, \( D_{loss} \) is the duty cycle loss.

\[
D_{loss} = D_p - D_s \tag{17}
\]

There are some reasons for the loss of the duty cycle: the transformer’s primary side current \( I_p \) needs time to conduct from positive to negative. During this period the transformer’s primary and secondary sides are decoupled. \( D_{loss} \) meets the following equation:

\[
D_{loss} = \frac{t_{sl}}{T_s} \tag{18}
\]

\[
t_{sl} = \frac{L_s[I_p(t_s) - I_s(t_s)]}{V_{in}} \tag{19}
\]

\[
D_{loss} = \frac{2L_s[I_p(t_s) - I_s(t_s)]}{V_{in} \cdot T_s} \tag{20}
\]

Time \( t_s, t_p \) and \( t_{sl} \) are expressed in Fig.2. To cope with the duty cycle loss, the saturated inductance solution is adopted here. The inductance grows to saturation when a large current flows through and exits saturation when the current drops [25].

C. Decision of \( Q_s \)’s Delay Time

As shown in Fig. 1, a secondary active clamp circuit has been added to the conventional PSFB converter to restrain the voltage overshoot. The driving signal of the clamp switch \( Q_s \) should synchronize with the rectifier’s output voltage \( V_{rec} \). Otherwise, \( V_{rec} \) will be affected and the peak value of \( I_p \) will increase. Considering that a PSFB converter with ZVS has a duty cycle loss on transformer’s secondary side, a \( \Delta t \) time-delay is needed to ensure that the clamp switch conducts before the arrival of \( V_{rec} \)’s rising edge. \( C_s \) has a linear charging current as shown in Fig.4. When the charging current \( I_c \) grows to zero, the voltage on the transformer’s secondary side \( V_{rec} \) reaches its midpoint. Therefore, it is determined that \( \Delta t \) meets equation (21)

\[
\Delta t \leq \frac{d}{4f_s} \tag{21}
\]

### Table I

<table>
<thead>
<tr>
<th>Converter Parameters</th>
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</thead>
<tbody>
<tr>
<td>Maximum input voltage</td>
</tr>
<tr>
<td>Maximum output voltage</td>
</tr>
<tr>
<td>Nominal output power</td>
</tr>
<tr>
<td>Switching frequency</td>
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### Table II

<table>
<thead>
<tr>
<th>Key Components</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>DSP</td>
<td>TMS320F2812</td>
</tr>
<tr>
<td>IGBTs(Q1-Q4)</td>
<td>F4-50R12KS4</td>
</tr>
<tr>
<td>IGBT (Qs)</td>
<td>FGL60N100BNTD</td>
</tr>
<tr>
<td>Diodes(D1-D4)</td>
<td>DSE60-12A</td>
</tr>
</tbody>
</table>

Fig. 9. A photo of the prototype (the converter’s PCB board is the same size as a sheet of A4 paper).

Where, \( d \) means the actual duty cycle of the voltage on the transformer’s secondary side. \( f_s \) means the switching frequency of the IGBTs in a PSFB converter.

V. EXPERIMENTAL RESULTS

The digital control core is a TMS320F2812 DSP. A 10kW IGBT-based prototype has been built with the parameters listed in Table I. The selections of the IGBTs and diodes are listed in Table II. The prototype is shown in Fig.9. To test the performance of the PSFB converter, a high power switching mode DC power supply, a high power resistor and a Tektronix MSO4034 oscilloscope were applied.

A. PSFB Converter’s Operation Properties

The driving waveforms of the converter are shown in Fig. 10. The switching frequency of the IGBTs is 20 kHz and the switching frequency of the clamp switch is 40 kHz. Fig. 11 shows the voltage and current waveforms of the transformer’s primary side. The current \( I_p \) and voltage \( V_{ab} \) trend is the same as the theoretical waveforms.
Fig. 10. Driving waveforms.

Fig. 11. Voltage and current waveforms of transformer’s primary and secondary side.

Fig. 12 depicts the effect of the secondary active clamp circuit. When the output voltage is 40V, the voltage overshoot and ringing effect on the rectifier bridge’s output side can be seen clearly in Fig. 12(a). After adding the secondary active clamp circuit, the waveform is smooth without spikes or oscillations as shown in Fig. 12(b).

The converter’s output waveforms are depicted in Fig.13. The converter firstly goes into the soft start. After that it is controlled by the closed-loop self-adaptive PI controller. As can be seen from Fig.13, the soft start-up lasts for 1.6 seconds and the whole start-up period is within 2 seconds without overshoots or vibrations.

The regulatory process of the conventional PI controller is about 160ms whereas that of the proposed PI controller is 97ms. The overshoot of the conventional PI controller is about 25%. However, there is hardly any overshoot with the propose PI controller. The good performance of the proposed PI controller is verified in many experiments. It has a faster respond speed, effectively suppressed vibrations and hardly any overshoot.

B. The Achievement of ZVS

Fig. 15 shows the waveforms of the ZVS. Fig. 15(a) shows the waveforms of the leading legs Q1 and Fig.15 (b) shows the lagging leg Q3. The waveforms of Q2 resemble Q1 and are neglected here. It is the same with Q4.

Fig.14 provides the dynamic response characteristics with the proposed self-adaptive PI controller, compared to a conventional PI controller under the same conditions.
As can be seen in Fig.15, the time allowance for the leading legs’ zero voltage turn-on is about 500ns and for the zero voltage turn-off it is about 200ns. The prototype achieves ZVS for the leading leg successfully which helps to reduce the switching loss and improve the converter’s efficiency remarkably. The lagging leg does not achieve zero voltage turn-on because the resonant inductor $L_{lk}$ is small and the load is light. However, it has an 800ns time allowance for the zero voltage turn-off.

C. The Converter’s Efficiency

The efficiency of the converter has been tested and sketched in Fig.16. The input voltage $U_{in}$ remained at 600V and the resistance load was 13Ω. The input current $I_{in}$ was read from the DC source and the output voltage $U_{o}$ was measured by a multi-meter. Finally the efficiency was calculated as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_o^2}{V_{in} \times I_{in} \times R}$$  \hspace{1cm} (22)$$

Fig. 16 shows an upward trend of the efficiency before 6.5kW and a downward trend after about 8kW. The lowest efficiency is 0.86 when the output power level is 0.75kW while the highest efficiency is 0.945 when power level reaches 8.2kW. The efficiency stays above 0.92 after 3kW. There is a decline in the efficiency after 8.2kW. The main reason for this may be due to the fact that the converter generates a great deal of heat.
VI. CONCLUSIONS

A digitally controlled phase-shifted full-bridge DC/DC converter using a secondary active clamp has been designed and implemented in this paper. The converter’s operation modes and the secondary active clamp circuit’s working modes have been analyzed. The features are verified by a 10-kW IGBT based prototype. Many advantages make this converter promising for high-voltage and high-power applications. Its distinctive advantages include:

1) Simple circuit topology.
2) Achieving ZVS for the leading and lagging legs without adding any lossy components.
3) The self-adaptive PI controller provides a faster respond speed, effectively suppressed vibrations and has hardly any overshoot.

There is much more to be done with this prototype such as reducing the heat produced by the converter.

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Yanbo Che was born in Shandong, China. He received his B.S. degree from Zhejiang University, Hangzhou, China, in 1993. He received his M.S. and Ph.D. degrees from Tianjin University, Tianjin, China, in 1996 and 2002, respectively. Since 1996, he has been engaged in teaching and scientific research of power electronic technology and power systems. He is presently an Associate Professor in the School of Electrical Engineering and Automation at Tianjin University. His current research interests include power electronics, new energy and micro-grids.

Yage Ma received his B.S. degree from the Nanjing University of Science and Technology, Nanjing, China, in 2012. Since September 2012, he has been working toward his M.S. degree at Tianjin University, Tianjin, China. His current research interests include switching power supplies.

Shaoyun Ge received his B.Sc. and M.Sc. degrees from Tianjin University, Tianjin, China in 1986 and 1991, respectively. He received his Ph.D degree in The Hong Kong Polytechnic University in 1998. Now he is a professor in Tianjin University.

Dong Zhu received his B.S. degree from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2010, and his M.S. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2013. His current research interests include switching power supplies.