DIMM-in-a-PACKAGE Memory Device Technology for Mobile Applications

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Abstract: A family of multi-die DRAM packages was developed that incorporate the full functionality of an SODIMM into a single package. Using a common ball assignment analogous to the edge connector of an SODIMM, a broad range of memory types and assembly structures are supported in this new package. In particular DDR3U, LPDDR3 and DDR4RS are all supported. The center-bonded DRAM use face-down wirebond assembly, while the peripherybonded LPDDR3 use the face-up configuration. Flip chip assembly as well as TSV stacked memory is also supported in this new technology. For the center-bonded devices (DDR3, DDR4 and LPDDR3 $\times 16$ die) and for the face up wirebonded $\times 32$ LPDDR3 devices, a simple manufacturing flow is used: all die are placed on the strip in a single machine insertion and are sourced from a single wafer. Wirebonding is also a single insertion operation: all die on a strip are wirebonded at the same time. Because the locations of the power signals is unchanged for these different types of memories, a single consolidated set of test hardware can be used for testing and burn-in for all three memory types.

Keywords: DRAM, multi-die package, ball assignment, wire bonding, system design

1. Introduction

A new multi-die memory module was developed for the Ultrabook™, Tablet and other portable applications requiring solder-down DRAM. In a single package, the entire functionality of an SODIMM was integrated. Key to this development was the design of a PCB layout-friendly universal ball-assignment scheme that supports DDR3, DDR4 and LPDDR3.

By constraining only the ballout and external mechanical dimensions, this DIMM-in-a-Package memory device can be constructed using several different assembly methods. For example assembly structures using wirebonded face-down, wirebonded face-up, flip-chip face-down and through-silicon-via (“TSV”) stacked-die using either a wirebonded or flipchip interface to the substrate can all be built in compliance with this new standard.

Manufacturing of the package is both simple and is low-cost: ordinary DRAM die are placed on the substrate strip using a single machine insertion and all of the die are wirebonded in a single machine insertion. From a strips-per-hour perspective the throughput and process flow is the same as Single-Die Packages (“SDP”) (Figure 1) in contrast with the flow for standard Double Die Packages (“DDP”) or Quad-Die Packages (“QDP”) (Figure 2), each of which

requires multiple passes through the assembly machinery, increasing cost by reducing manufacturing throughput. But the cost savings don't end there: the standard DDP and QDP devices also use a costly ReDistribution Layer (“RDL”) to relocate the bonding pads to the edge of the die to facilitate stacking of the wire-bonded die. RDL is both expensive and has poor electrical properties: it has resistance and inductance that adversely affects the Power Integrity (“PI”) and has additional capacitance that degrades switching performance and Signal Integrity (“SI”). The DIMMin-a-PACKAGE memory devices have no such demerits.

A comparison of relative costs of assembly for the SDP, RDL-Spacer QDP, Stairstep RDL QDP and the DIMM-in-

Fig. 1. Manufacturing process flow for DIMM-in-a-PACKAGE memory devices.

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Fig. 2. Manufacturing process flow for conventional DDP and QDP memory devices.

Table 1. Assembly cost (exclusive of die and test costs) for Invensas QFD™ DIMM-in-a-Package memory devices compared to conventional wirebonded four-die packages.

Device	Relative Cost
Single Die Package	1.0×
Invensas QFD™	3.7×
Stairstep RDL QDP	7.8×
RDL Spacer QDP	8.4×

a-PACKAGE memory device is listed in Table 1. All costs exclude die cost (but include RDL cost where required) and testing cost and all are normalized to SDP cost.

2. Ball Assignment Design

The ball assignment was designed for simplicity of the PCB layout when using Type 3 PCBs and to support DDR3, DDR4 and LPDDR3 devices in a common package ballout. A key feature of the ball assignment is the mirror image symmetry of the signals about the Y-axis. Not only are the DQ signals and CA signals symmetric, the power signals are as well. The symmetry offers the PCB layout engineer a very simple way to make a double-sided clamshell layout: the active signals and power connections that must be interconnected to devices placed on opposite sides of the board, simply are connected together using vias that pass through the board. The result was that data signals landed atop data signals, data strobes landed atop data strobes and so on.

Since the CA signals balls are assigned to the balls placed in center of the package, the symmetry was maintained by creating a duplicate set of CA signals with both sets disposed in the central region in a mirror image about the Y axis. The duplicate CA signal set offered several advantages

1) The substrate design was simplified: each CA signal was only connected to two die rather than to all four

2) The mirror-imaged dual CA bus is simple to interconnect when the devices are used as a dual rank placed in clamshell configuration: each CA signal of the top side device lands atop an identical signal on the bottom side device. The result is an ultra-simple and clean layout

3) The dual CA bus permits each pair of devices to be operated independently: the DIMM-in-a-PACKAGE memory device can be operated as a single ×64 channel or as two separate 32 bit channels. The latter configuration is designed for supporting the needs of the Tablet market which uses dual 32 bit memory channels, while the former is designed for the Ultrabook processor which has 64 bit dual memory channels.

3. Test Hardware Consolidation

Test hardware can be a costly manufacturing infrastructure investment. The major expense items are the HIFIX (Load board / test sockets) for the high speed testers and the Burn-In boards needed for the burn-in ovens. Depending on the testers involved and the number of parallel channels used, a HIFIX for a single tester will cost \$500K USD to \$800K USD. Burn-in boards to fill an entire burn-in oven can cost \$125K to \$250K. Additional capacity implies additional copies of these boards to be purchased.

All of the switching signals can be programmed by the Automatic Test Equipment (“ATE”) but power supply signals must be hard-wired in the test boards. As a result, changing even one power pin means all the boards must be scrapped and replaced at great expense.

One of the very attractive aspects of the DIMM-in-a-PACKAGE memory technology is that the ball assignment is compatible for DDR3, DDR4 and LPDDR3. As a result a single set of test hardware can be developed and used to support all three device types. The savings for a high-volume production facility can be millions of dollars.

4. System Design

Recently introduced notebook and tablet PCs feature very thin cases. The form-factors of these products do not support conventional SODIMM type memory modules. Instead DRAM is soldered directly to the system motherboard to minimize the XYZ dimensions of the electronics.

A first generation product using this “solder-down” memory configuration used conventional single die DRAM packaging on a double-sided PCB assembly based on High Density Interconnect (“HDI”) technology configured as a 3-6-3 stackup.

Fig. 3. (a) “Type 4” PCB: HDI Printed Circuit Board (12 layer: 3-6-3, Blind and Buried Vias) (b) “Type 3” Standard Process PCB (12 layer).

HDI PCB technology provides blind via structures (Figure 3a). These vias do not pass completely through the board. This allows very high density interconnections to be made compared to standard process PCBs using vias that pass completely through the PCB (Figure 3b).

The CPU-memory channel layout was one of three regions that forced the use of HDI technology. The other two were the packaging used for the peripheral control hub and for the embedded controller: both required HDI for the package breakout due to aggressive ball pitch (500 microns) or interdigitated ball placements with fine pitch.

Each of these components is offered in packaging that doesn't require HDI for breakout, but those packages require a larger footprint on the PCB and would not fit into the PCB area budget when using SDP DRAM.

For the CPU-memory channel layout, two factors forced the use of HDI. The first was the ball assignment of the industry standard DRAM packaging prevented direct sharing of facing terminals on DRAM packages mounted on opposite sides of the PCB. Double-sided placement was required by the area constraints of the PCB.

The second was a requirement for serpentine routing throughout the memory channel region to satisfy minimum trace length requirements imposed by electrical design rules. The large number of vias needed for double-sided SDP DRAM breakout routing blocked routing channels, complicating the use of serpentine routing required for design rule compliance.

The blind via technology provided by HDI PCB manufacturing processes permitted the memory channel's layout area budget constraint to be met when using SDP DRAM, but at high cost.

A key goal of this work was to develop a memory channel solution based on custom packaging to replace the HDI technology with low-cost common multilayer plated-through-hole-via glass-epoxy PCB technology while meeting

form-factor and performance requirements.

5. Feasibility Study

To illustrate the advantages offered by the DIMM-in-a-PACKAGE memory technology, a redesign of a first generation Ultrabook product was undertaken. The memory and CPU portions of the design were redesigned to use the newly developed package concept and the entire design was converted to a Type 3 PCB of 12 layers.

The original design used two memory channels made from 2 Gbit DDR3 $\times 8$ DRAM organized as a single rank. The new design was also a dual channel design but used two ranks of $\times 16$ organized die placed into an early version of the DIMM-in-a-PACKAGE device package. Although the ball assignment and physical size of this early prototype device was different than the Plan Of Record (“POR”) device, the key features of the device were the same:

- 1) Four $\times 16$ organized DDR3 devices in a single package
- 2) Mirror symmetry about the Y axis
- 3) Dual CA bus balls arranged in a mirror image symmetry about the Y axis

6. Reference Design: SDP Memory With HDI (12 layer: 3-6-3) TYPE-4 PCB

The CPU and memory region of the reference design is shown in Figure 4. The PCB fabrication technology was 12-layer HDI TYPE 4 technology using a 6 layer core with three build-up layers on either side (3-6-3 HDI). SDP DRAMs were used on the design and placed on both sides of the PCB and co-aligned.

6.1. Cost-Reduced Design: Standard Process PCB (12 Layer PTH vias)

The cost-reduced design was based on an early version of the DIMM-in-a-PACKAGE memory device. The package

Fig. 4. 12-layer (3-6-3) HDI PCB Implementation using Single Die Packages (yellow lines included for size comparison reference).

Fig. 5. Quad Face Down Wirebonded DDR3 version of the DIMM-in-a-PACKAGE memory device.

used had 240 balls arranged in a 17×17 mm footprint. The POR device package features the same design considerations but is larger so as to accommodate the additional signals and power pins necessary to co-support DDR4, LPDDR3 and DDR3 in the same package. The final footprint size of the POR device is 17.5×22.5 mm while the thickness is 1.0 mm for the production version. A photograph of the package is shown in Figure 5. The substrate layout for the DDR3 version is shown in Figure 6.

The original HDI-based design was converted to a non-HDI (Type 3) PCB using the same number of layers as before. However the area needed for the memory subsystem was 40% less than required for the HDI implementation using SDPs. The area reduction allowed the larger footprint PCH and EC to be used, which do not require HDI for breakout routing. The new design is shown in Figure 7. The dashed yellow lines are placed in the middle of the CPU's thermal mounting holes to provide a convenient visual reference to show the two PCBs are displayed at the same scale.

The major benefits were:

- 1) PCB cost reduced to 20% of HDI
- 2) Prototypes in 5 days vs 3 weeks for HDI

Fig. 6. Substrate layout for the DDR3 version.

Fig. 7. 12 Layer Standard Process Type 3 PCB implementation using Quad Die Package with Invenas Ballout.

7. Details: Comparison of Memory Footprint Layouts

A comparison of the layout of the memory package footprint breakout regions for the two different PCB designs is shown in Figure 8. In these views the top and bottom routing layers plus vias are shown for both designs. Figure 8 left shows two die in the basic SDP footprint (two sided assembly) fabricated using HDI, while Figure 8 right shows eight die in the QFD footprint fabricated using the normal process PCB.

A close examination reveals that none of the vias needed for the SDPs are shared but most of the vias needed for the new package are shared. This is one of the key reasons why this new package ballout can be used on ordinary PCBs featuring through-board vias. But there is additional benefit: shared vias minimize breakout stub lengths, improving high speed signal integrity without costly HDI.

The length of the stubs interconnecting same-named signals in the C/A region for the SDP PCB layout are several millimeters long and of variable length. These stubs affect the signal integrity for the C/A bus and play a role in establishing the upper operating frequency of the memory subsystem. By comparison, the double set of C/A bus signals arranged into two mirror-imaged columns requires no cross-tie connections. The result is the stub lengths required for interconnecting the two oppositely-placed packages are essentially the thickness of the PCB, a significant improvement attained on a much lower-cost PCB. The electrical advantages of this interconnection scheme will be of significant benefit when memory devices convert the C/A signals to double edge clocking as is a feature of LPDDR3.

Fig. 8. Breakout region comparison: original Type 4 HDI version (left) and new Type 3 version (right).

Fig. 9. Variety of assembly and memory technologies supported by common ballout.

8. Features and Versatility of Ballout

The ballout developed for the new quad die facedown package has features that accommodate its specific mechanical requirements. The depopulated square ring is one such feature. But the ballout is not limited solely to the face down wirebonded quad die structure.

For example a stacked arrangement of face up periphery-bonded die such as LPDDR3 separated by spacer die can be readily supported by this ballout. Likewise one or more flip-chip die can also be supported by the ballout. Even proposed master-slave TSV die stacks(2) can be supported by this versatile ballout. Figure 9 shows various structures that can use this ballout technology.

An interesting feature of the ballout is that it can enable a unified PCB design for controllers that offer co-support of DDR3 and LPDDR3. Because LPDDR3 and DDR3 have identical signals on the “data side”, its requirements are easily met using the signal assignment of the outer region of the new ballout.

LPDDR3 differs from DDR3 on the address/command side. Instead of sampling these signals on the rising edge of the clock only, LPDDR3 samples a smaller number of signals on both edges of the clock to extract the address and command information.

A controller that offers co-support of DDR3 and LPDDR3 will simply multiplex the LPDDR3 CA signals onto the existing DDR3 C/A bus signals using a particular mapping onto the PHY's DDR3 C/A signals. By duplicating that mapping for the new memory ballout, a PCB can be designed that will accommodate either DDR3 or LPDDR3 using the same PCB raw card when using this universal ballout with controllers featuring LPDDR3/DDR3 co-support. Full details of this scheme will be described in a paper submitted to ISQED2013 scheduled to be presented in March 2013 in Santa Clara, California.

9. Conclusion

New ultra-slim form factors for portable client computers

have displaced the SODIMM in favor of soldered-down memory on the motherboard. Current systems primarily use conventional single die DRAM packaging on costly HDI PCBs to meet PCB formfactor and electrical design constraints.

A new quad die DRAM packaging technology was developed to simplify the design challenges for this new class of client computers. Coupled with a versatile and efficient ballout this package eliminates the requirement for HDI PCB technology by providing a layout-friendly ballout that allows via-sharing for double-sided component assemblies.

Besides supporting quad-die low-cost wirebonded DDR3 memory die, the ballout also supports many other types of memory die and package configurations including LPDDR3

permitting a common PCB design to support either type of DRAM providing maximum configuration flexibility for the system OEM.

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