Progress of High- k Dielectrics Applicable to SONOS-Type Nonvolatile Semiconductor Memories

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As a promising candidate to replace the conventional floating gate flash memories, polysilicon-oxide-nitride-oxide-silicon (SONOS)-type nonvolatile semiconductor memories have been investigated widely in the past several years. SONOS-type memories have some advantages over the conventional floating gate flash memories, such as lower operating voltage, excellent endurance and compatibility with standard complementary metal-oxide-semiconductor (CMOS) technology. However, their operating speed and data retention characteristics are still the bottlenecks to limit the applications of SONOS-type memories. Recently, various approaches have been used to make a trade-off between the operating speed and the data retention characteristics. Application of high- k dielectrics to SONOS-type memories is a predominant route. This article provides the state-of-the-art research progress of high- k dielectrics applicable to SONOS-type nonvolatile semiconductor memories. It begins with a short description of working mechanism of SONOS-type memories, and then deals with the materials' requirements of high- k dielectrics used for SONOS-type memories. In the following section, the microstructures of high- k dielectrics used as tunneling layers, charge trapping layers and blocking layers in SONOS-type memories, and their impacts on the memory behaviors are critically reviewed. The improvement of the memory characteristics by using multilayered structures, including multilayered tunneling layer or multilayered charge trapping layer are also discussed. Finally, this review is concluded with our perspectives towards the future researches on the high- k dielectrics applicable to SONOS-type nonvolatile semiconductor memories.

Keywords: High- k dielectrics, Polysilicon-oxide-nitride-oxide-silicon, Nonvolatile semiconductor memories

1. INTRODUCTION

According to the Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) [1], the scaling of tunneling layer is a key issue for the conventional floating gate-type nonvolatile semiconductor memories (FG-NVSM) and new flash NVSM technology will be required to achieve reliable, low-power, low-voltage performance in the future. The conventional floating gate-type flash nonvolatile

semiconductor memory will suffer from the stress-induced leakage current (SILC) issue due to adopting the ultra-thin tunneling oxide. As one of the most promising candidate to replace the conventional floating gate-type flash nonvolatile memory, the charge trapping-type nonvolatile semiconductor memory, have received much attention due to their advantages over the conventional floating gate-type flash nonvolatile memory, such as low programming voltage, low power, excellent endurance and compatibility with standard complementary metal-oxide-semiconductor (CMOS) technology [2]. The charge trapping-type NVSM devices can be mainly classified as three types [3-11]: polysilicon-oxide-nitride-oxide-silicon (SONOS), nitride-base

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Fig. 1. Schematic diagrams of two types of memory devices: (a) floating gate; (b) polysilicon-oxide-nitride-oxide-silicon (SONOS).

read-only-memory (NROM) and nanocrystal memory (NCM). The NROM have better data retention characteristic than SONOS/MONOS devices due to adopting thicker tunneling layer. However, the NROM utilize hot carrier injection for write and erase, in which large power is consumed during the operation. Meanwhile erase saturation and vertical stored charge migration [12-14], which can degrade the performance of device, are also the major drawbacks for NROM devices. As for the NCM device, to control the size, density and uniform distribution of nanocrystals are extremely challenging issues [15]. In the SONOS devices, thin silicon dioxide is typically used as the tunneling layer, since it has high operating speed, low write/erase voltage and superior endurance. However, the data retention time [16-18] and program/erase speed are still the bottlenecks for the applications of SONOS due to the thin tunneling layer [19]. SONOS devices evolve from traditional metal-nitride-oxide-silicon (MNOS) devices [20] that pioneered in the history of nonvolatile semiconductor memory in 1960's. Up to date, various approaches have been used to gain a trade-off between the data retention time and the program/erase speed, to solve the issue of scaling conventional floating gate [21-23] during the continuous reduce of the device size. Among which, application of high-*k* dielectrics to SONOS-type memories is a predominant route. In this work, we will provide a comprehensive review of the recent research progress of high-*k* dielectrics applicable to SONOS-type nonvolatile semiconductor memories. This review is organized as follows: it begins with a short description of working mechanism of SONOS-type memories, and then highlights the materials' requirements of high-*k* dielectrics used for SONOS-type memories. In the following section, microstructures of high-*k* dielectrics used as tunneling layers, charge trapping layers and blocking layers in SONOS-type memories, and their impacts on the memory behaviors are critically reviewed. The improvement of the memory characteristics by using multilayered structures,

Table 1. Some requirements for high-*k* materials.

	Requirements	Remarks
High- <i>k</i> materials	High dielectric	Not the larger the better [42-44]
	Enough barrier height and large band gap	Reduce the leakage current [45]
	Thermodynamically stable with Si substrate	Most high- <i>k</i> materials form interface layer
	Amorphous state under high temperature	Grain boundary can act as current leakage paths [46]
	Compatible with conventional CMOS technology	

Table 2. Performance comparison of some high-*k* materials [47].

Material	Dielectric constant (<i>k</i>)	Band gap E_g (eV)	ΔE_c (eV) to Si	Crystal structure
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2.4	Amorphous
Al ₂ O ₃	9	8.7	2.8	Amorphous
TiO ₂	80-100	3.5	1.2	Tetragonal
Ta ₂ O ₅	26	4.5	1-1.5	Orthorhombic
HfO ₂	25	5.7	1.4	Mono., tetrag., cubic
ZrO ₂	25	7.8	1.5	Mono., tetrag., cubic
La ₂ O ₃	30	4.3	2.3	Hexagonal, cubic
Y ₂ O ₃	15	5.6	2.3	Cubic
Gd ₂ O ₃	24 ± 2			
Er ₂ O ₃	14.4	7.5	3.5	
Nd ₂ O ₃		5.8	2.2	
PrO ₂	25	3-4	>1	Cubic
CeO ₂	52, 26	4.5		

including multilayered tunneling layer or multilayered charge trapping layer are also discussed. Finally, this review is concluded with our perspectives towards the future researches on the high-*k* dielectrics applicable to SONOS-type nonvolatile semiconductor memories.

2. MECHANISM OF CHARGE STORAGE

Figure 1 shows the schematic diagrams of the floating gate memory and the SONOS type memory, respectively. In the conventional floating gate-type flash nonvolatile memory, a single defect can discharge the stored charge of the device due to the conductive properties of the floating polysilicon gate electrode. For the case of the SONOS type memory device, however, the charges are stored in discrete traps, since a single defect will not cause the discharge of the whole memory. During the program operation, when a positive gate voltage is applied to the gate electrode relative to the p-Si substrate, the inversion layer form. Electrons tunnel through the tunneling layer into the charge trapping layer and result in a positive threshold voltage shift under the effect of electric field. On the contrary, during the erase operation, holes are injected from p-Si substrate into the charge trapping layer where they are trapped in a manner similar to electrons and lead to a negative threshold voltage shift.

In the past several decades, many efforts have been made to find new materials, structures and technologies in order to meet the requirements, such as low voltage (<5 V), low power programming with long-term retention (>10 years at 85°C) and endurance (>10⁶ write/erase cycles) performance [24]. Employing the high dielectric constant (high-*k*) materials to replace the sili-

Fig. 2. Predicted band offsets for various high- k oxides [47].

Fig. 3. Leakage current characteristics of metal-hafnium-oxide-semiconductor capacitors with various thicknesses of HfO_2 layer. Inset shows tunneling current characteristics of metal-nitride-oxide-silicon capacitors with various thicknesses of Si_3N_4 layer [58].

con dioxide or silicon nitride in the traditional SONOS/MONOS-type devices is a predominant approach.

3. MATERIALS' REQUIREMENTS

In the semiconductor industry, the requirements for high density and low cost have driven the continuous scaling in the dimensions of metal-oxide-semiconductor field effect transistors (MOSFETs) [25]. However, as the thickness of SiO_2 gate dielectrics approaches to 2-3 nm, high leakage current becomes as serious obstacles to future device reliability [26]. In order to overcome these problems, higher permittivity (k) materials, which allows an equivalent capacitance to be achieved using a physically thicker insulating layer, can replace the conventional SiO_2 gate dielectric to realize further scaling down. Therefore, in the past several years, much attention have been given to alternative high- k dielectric oxides such as silicates (e.g., Zr and Hf silicate [27, 28]), single metal oxides (e.g., HfO_2 [29], ZrO_2 [30], Al_2O_3 [31], La_2O_3 [32], Pr_2O_3 [33], Y_2O_3 [34], Gd_2O_3 [35], Nd_2O_3 [36]), and binary metal oxides [37-40]. In order to meet the requirements of CMOS field effect transistors, the high- k dielectrics should satisfy some requirements, as summarized in the Table 1 [41].

The performance comparison and the predicted band offsets of some high- k dielectrics are given in Table 2 and Fig. 2,

Fig. 4. Transmission electron microscopy images of $\text{HfO}_2/\text{SiO}_2$ layers on Si substrates. (a) $\text{HfO}_2 = 8$ nm and (b) $\text{HfO}_2 = 2$ nm [58].

respectively. In the conventional SONOS devices, the poor data retention time and the slow program/erase speed are the bottlenecks to limit their applications. The program/erase speed can be enhanced by scaling the tunneling layer thickness. However, the data retention capability becomes worse simultaneously due to the reduction of tunneling layer thickness [48]. To solve this issue, the high- k dielectrics have been investigated widely to obtain a trade-off between the operating speed and the data retention time for SONOS devices.

4. MEMORY CHARACTERIZATION

As an important charge trapping nonvolatile semiconductor memory, SONOS-type devices employ a charge trapping layer to replace the conventional floating gate. However, the conventional Si_3N_4 charge trapping layer has lower trap density, it cannot meet the requirements of scaling down the charge trapping memories in the future. In addition, traps are considered to originate from defects present in the charge trapping layer, which capture electrons or holes. However, only a certain traps can store charges and maintain a stable memory characteristic after programming, which are considered as effective traps for memory application [49]. To increase the trap densities and to store more charges, adopting high- k dielectrics in the SONOS-type memory devices becomes as the predominant approach in the past decades. Up to now, the dominant approach can be subdivided into the following fields: (a) high- k dielectrics as charge trapping layer, (b) high- k dielectrics as charge trapping layer and blocking layer, (c) high- k dielectrics application to three layers, and (d) multilayered structures.

Fig. 5. C-V measurements of the $Ti_{0.25}Al_{0.75}O_x$ capacitors measured at 1 MHz and annealed at (a) 800°C and (b) 900°C, respectively [61].

4.1 High- k dielectrics served as the charge trapping layer

Silicon nitride as the charge trapping layer in the SONOS devices have been studied extensively and the results showed that the devices have poor data retention and scaling issue [50]. The high- k materials such as Al_2O_3 , La_2O_3 , ZrO_2 , and HfO_2 in a metal-oxide-high- k -oxide-silicon structure are reported [51-54]. HfO_2 , as the most promising candidate for SONOS devices, has attracted much attention because of its good thermodynamical stability with Si, high dielectric constant, and relatively large band gap (~ 5.68 eV) [55]. Zhu *et al.* [56, 57] reported on the electrical properties of HfO_2 as the gate dielectric deposited by pulse laser deposition. You *et al.* [58] deposited HfO_2 films with various thickness by atomic layered chemical vapor deposition to replace Si_3N_4 as the charge trapping layer and formed metal-hafnium-oxide-semiconductor (MHOS) structure. Figure 3 shows the leakage current characteristics MHOS memory capacitors with various thicknesses of HfO_2 layer. The data demonstrated that employing stack HfO_2 charge trapping layer could decrease the leakage current as compared with a single SiO_2 layer. However,

Fig. 6. Cross-sectional high-resolution transmission electron microscopy images of the $Ti_{0.25}Al_{0.75}O_x$ films annealed at (a) 800°C and (b) 900°C [61].

the leakage current for the applied electric field is almost the same irrelevant to the thickness of HfO_2 charge trapping layer. Inset in Fig. 3 shows the leakage current characteristics of MNOS capacitors with various thicknesses of Si_3N_4 layer, which indicated that the leakage current of device was reduced by utilizing the HfO_2 films as the charge trapping layer and it could obtain larger memory window than the Si_3N_4 at same trapping layer thickness. The transmission electron microscopy (TEM) images of HfO_2/SiO_2 stacked layers as charge trapping layer/tunneling layer of MHOS structure capacitors, is shown in Fig. 4. From which, an abrupt interface between the HfO_2 layer and SiO_2 layer was clearly observed.

Fig. 7. Comparison of schematic energy band diagram for the conventional SONOS (dashed line) structure and the SHNOS (solid line) structure at the write mode (a) and erase mode (b) [62].

Pan and Yeh [59, 60] also reported a novel high-*k* SONOS structure using Y_2O_3 as charge trapping layer. This structure had long charge retention characteristic due to deep trap level and excellent endurance. The group also demonstrated the MONOS-type memory device using the high-*k* NdTiO_3 as the charge trapping layer. They deposited ~6 nm Nd_2O_3 film and ~6 nm Ti film on SiO_2 in turn by reactive radio frequency (RF) sputtering. The NdTiO_3 film was formed by rapid thermal annealing (RTA) in O_2 ambient at various temperatures for 30 seconds. The NdTiO_3 MOHOS-type memories have small charge loss rate due to the deep trap levels in high-*k* layer [48]. Shi *et al.* [61] found that the pseudo-binary $\text{Ti}_{0.25}\text{Al}_{0.75}\text{O}_x$ film as the gate dielectric exhibited a characteristic of electrical hysteresis after high-temperature treatment. Figure 5 showed the C-V electrical hysteresis curves for pseudo-binary $\text{Ti}_{0.25}\text{Al}_{0.75}\text{O}_x$ films. As shown in Fig. 5, the width of the hysteresis window derived from the $\text{Ti}_{0.25}\text{Al}_{0.75}\text{O}_x$ film annealed at 900°C was much larger than that annealed at 800°C. The phenomenon could be mainly ascribed to the oxygen vacancies created easily at low oxygen partial pressure. Furthermore, the ionization of oxygen vacancies will create conducting

Fig. 8. High-resolution transmission electron microscopy image of a high-*k* HfO_2 charge trapping layer with high-*k* Al_2O_3 as a blocking oxide for a memory capacitor [63].

Fig. 9. Flat band voltage versus time of SONOS-type memory devices with Si_3N_4 , Al_2O_3 , HfO_2 , or HfAlO as the charge trapping layers [69].

electrons and these electrons can be combined with Ti^{4+} ions to reduce them to Ti^{3+} ions and/or trapped in oxygen vacancies in turn and lead a positive V_{FB} shift. Therefore, the high-*k* $\text{Ti}_{0.25}\text{Al}_{0.75}\text{O}_x$ films have promising applications as charge trapping layers. The cross-sectional high-resolution TEM (HRTEM) images of the films annealed at 800°C and 900°C were shown in Fig. 6. Clearly, the $\text{Ti}_{0.25}\text{Al}_{0.75}\text{O}_x$ films still remained amorphous state after 800°C annealing, whereas in the films annealed 900°C several crystal regions were obviously observed. The traps in these crystal regions could capture the charges.

Fig. 10. Cross-sectional transmission electron microscopy images for the memory structures with (a) untreated and (b) nitrided tetragonal ZrO_2 films [72].

4.2 High- k dielectrics served as the charge trapping layer and blocking layer

Accordingly, the considerable charge loss through the ultra-thin tunneling layer for SONOS/MONOS devices is the formidable obstacle. Lee et al. [62] reported on a new $\text{SiO}_2/\text{SiN}/\text{Al}_2\text{O}_3$ structure that can obtain fast operating speed by Fowler-Nordheim tunneling mechanism. This structure allowed a thicker tunneling layer over 3 nm. The schematic energy band diagram for this structure is shown in Fig. 7. The following equations are used to explain the benefit of this structure under erase mode.

$$E_{TL} = \frac{|V_g| - \phi_{ms} - \phi_s - \frac{Q_{CTL}}{\epsilon_0} \left(\frac{x_{BL}}{\epsilon_{BL}} + \frac{x_{CTL}}{2\epsilon_{CTL}} \right)}{x_{TL} + \frac{\epsilon_{TL}}{\epsilon_{CTL}} x_{CTL} + \frac{\epsilon_{TL}}{\epsilon_{BL}} x_{BL}} \quad (1)$$

$$E_{BL} = \left(E_{TL} + \frac{Q_{CTL}}{\epsilon_0 \epsilon_{TL}} \right) \frac{\epsilon_{TL}}{\epsilon_{BL}} \quad (2)$$

Where E_{TL} and E_{BL} are the electric fields across tunneling layer and blocking layer, respectively. V_g is the erase gate voltage, ϕ_{ms} is the work function difference between the gate and the silicon substrate, ϕ_s is the surface potential, Q_{CTL} is the total amount of the charge trapped in the charge trapping layer, ϵ_{CTL} , ϵ_{TL} and ϵ_{BL} are the dielectric constants in the charge trapping layer, the tunneling layer and blocking layer, and x_{CTL} , x_{TL} and x_{BL}

Fig. 11. Comparison of the retention characteristics at 125°C for the memory devices with and without nitridation of the tetragonal ZrO_2 films [72].

Fig. 12. Cross-sectional transmission electron microscopy image of the $\text{SiO}_2/\text{HfO}_2\text{-Al}_2\text{O}_3\text{-HfO}_2$ (HAH)/ $\text{Al}_2\text{O}_3/\text{HfN}$ memory capacitor [86].

are the thickness of the charge trapping layer, tunneling layer and blocking layer, ϵ_0 is the permittivity of free space. By using blocking materials with higher dielectric constant than the tunneling layer, the value of E_{TL} was enhanced, and the E_{BL} was suppressed simultaneously. The results lead to a high operating speed even at a thicker tunneling layer and small gate injection current.

Maikap et al. [63] measured the charge trapping characteristics of p-Si/ $\text{SiO}_2/\text{HfO}_2/\text{Al}_2\text{O}_3$ /metal memory structures. A large memory window of 7.4 V and a high charge trapping density of $1.1 \times 10^{13} \text{ cm}^{-2}$ were reported on the high- k HfO_2 charge trapping memory capacitors. These capacitors were treated by RTA at 1,000°C for 10s in N_2 ambient. A typical HRTEM image of a high- k HfO_2 charge trapping layer with high- k Al_2O_3 as a blocking oxide for the memory capacitor, is shown in Fig. 8, in which the

Fig. 13. Transmission electron microscopy images of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ (ONO) and $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}_3\text{N}_4$ (NON) tunneling layers with HfO_2 as charge trapping layer and Al_2O_3 as blocking layer [88].

HfO_2 film is polycrystalline, whereas the Al_2O_3 film as a blocking oxide is almost amorphous.

In recently years the $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ films as the promising materials are investigated widely [64-68]. Tan *et al.* [69] used the HfAlO , Al_2O_3 and Si_3N_4 films as the charge trapping layers to comparatively investigate the retention performance of memory devices. In addition, they used HfAlO films with different compositional ratios of HfO_2 to Al_2O_3 as a blocking layer, and tested the memory characteristics. The retention characteristics of memory devices with different charge trapping layers were showed in Fig. 9. Clearly, the memory devices with HfO_2 as the charge trapping layer exhibited the worst data retention characteristics. The HfAlO -based memory devices have a similar data retention performance to that based on Si_3N_4 , but they are slightly worse than Al_2O_3 . The use of HfAlO films with different compositional ratios of HfO_2 to Al_2O_3 instead of the conventional SiO_2 as the blocking layer, results in an increase of the program and erase

Fig. 14. (a) High-resolution transmission electron microscopy (HR-TEM) image of high-k HfO_2 (0.5 nm)/ TiO_2 (0.5 nm) multilayers with ten periods in $\text{p-Si}/\text{SiO}_2/(\text{HfO}_2/\text{TiO}_2)/\text{Al}_2\text{O}_3$ structure after annealing at 900°C for 1 minute in N_2 ambient. (b) HRTEM image with elemental line profile by DIGITAL MICROGRAPH software shows the clear $\text{HfO}_2/\text{TiO}_2$ layer-by-layer structure (red color) [89].

speeds, especially at low gate voltages. Pu *et al.* [70] also studied the charge trapping flash memory with $(\text{Gd}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}$ films as blocking layers. Their experimental results demonstrated that the doping of Al into pure Gd_2O_3 film was an effective way to improve the charge retention of SONOS-type nonvolatile memory, and that 35 mol% Al was the optimized Al concentration in $(\text{Gd}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}$ films. Park *et al.* [71] further examined the memory characteristics with three different films (Al_2O_3 , Gd_2O_3 and $(\text{Gd}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}$) as the blocking layers. Their results demonstrated that addition of Gd into Al_2O_3 reduced the leakage current, and improved the erase window. The crystallization of the $(\text{Gd}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}$ films leads to a change in the band gap of the $(\text{Gd}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}$ film, resulting in a change of the retention properties.

Wu *et al.* [72] also investigated the memory characteristics of metal/insulator/metal (MIM) capacitors with NH_3 nitrided tetragonal ZrO_2 film as the charge trapping layer and Al_2O_3

Table 3. Performance comparison of MATHS and MHTHS structure [74].

Structure	Speed ($V_{TH} > 0.5V$)	20% charge loss(s)	Initial memory window/after ten years (V) (85°C)	Date endurance after 10^5 cycles
MATHS	100 ns@10 V	75	2.5/1.41	Excellent endurance performance
MHTHS	1 μ s@10 V	50	0.9/0.42	Excellent endurance performance

MATHS: TaN/Al₂O₃/Ta₂O₅/HfO₂/Si, MHTHS: metal/HfO₂/Ta₂O₅/HfO₂/Si.

blocking layer. Figure 10 shows the cross-sectional TEM images of the memory structures with nitrided tetragonal ZrO₂ film and untreated tetragonal ZrO₂ film as the charge trapping layer. After nitridation, the physical thickness was found to be still kept intact. The data retention characteristics (at 125 °C) of the memories with and without NH₃ nitridation of the tetragonal ZrO₂ film, is shown in Fig. 11. As shown in Fig. 11, the nitride tetragonal ZrO₂ films have better data retention and hold the great potential for future high-performance nonvolatile memory, as compared with the tetragonal ZrO₂ films without nitridation.

4.3 High-*k* dielectrics served as the tunneling layer, the charge trapping layer and blocking layer

In the future, scaling tunneling layer and ten-year retention requirement at the same time are the key issues to the SONOS-type nonvolatile semiconductor memories. Therefore, looking for new high-*k* materials to replace the tunneling layer is an important subject. Wang *et al.* [73] fabricated a novel metal/HfO₂/Ta₂O₅/HfO₂/Si (MHTHS) structure, which had a 1 μ s programming speed and 1 ns erasing speed. Wang and Kwong [74] also employed the TaN/Al₂O₃/Ta₂O₅/HfO₂/Si (MATHS) structure to obtain fast speed and long retention characteristic. Their experimental results demonstrated that the memory window and programming speed were improved by using Al₂O₃ to replace HfO₂ as the blocking layer. Table 3 presents the performance comparison between the MATHS and MHTHS structures.

4.4 Multilayer structure

The multilayer tunneling layer concept seems to be a promising route to achieve a trade-off between the operating speed and the date retention due to the redistribution of electric field across the multilayer tunneling layer compared with a single tunneling layer, making the tunneling layer thinner at the same applied bias [75–84]. Chen *et al.* [85] fabricated a memory capacitor with a multistacked tunneling layer of Al₂O₃/HfO₂/SiO₂ (AHO) together with HfO₂ charge trapping layer and Al₂O₃ blocking layer. As compared to a single SiO₂ tunneling layer, the multistacked tunneling layer, can offer a large memory window (7.6 V) for ± 12 V sweep voltage range and an improved date retention characteristic. Ding *et al.* [86] also reported on a novel multilayered structure of SiO₂/HfO₂-Al₂O₃-HfO₂ (HAH)/Al₂O₃/HfN as the charge trapping layer, where HAH multilayer possess of better thermal stability and higher charge storage capability compared to pure HfO₂ film [87]. A cross-sectional TEM image of the SiO₂/HAH/Al₂O₃/HfN memory capacitor, is shown in Fig. 12, and sharp interfaces within the Si/SiO₂/HAH/Al₂O₃/metal structure are clearly observed. This memory capacitor exhibits a sufficient electron and hole trapping efficiencies such as an electron density of $\sim 7 \times 10^{12}$ cm⁻² under 13 V program for 0.5 ms and a hole density of $\sim 4 \times 10^{12}$ cm⁻² under -12 V erase for 0.5

ms. Park and Cho [88] fabricated charge trapping type memory with SiO₂/Si₃N₄/SiO₂ (ONO) and Si₃N₄/SiO₂/Si₃N₄ (NON) multilayer structure as the tunneling layers, respectively. Then the HfO₂ and Al₂O₃ films were deposited by atomic layer deposition as the charge trapping layer and blocking layer. Figure 13 show the TEM images of ONO and NON tunneling layers with HfO₂ as charge trapping layer and Al₂O₃ as blocking layer. The experimental results demonstrated that adopting the ONO structure as the tunneling layer has not only long data retention time but also superior endurance characteristics. However, the NON tunneling layer showed degraded retention and endurance characteristics due to the program/erase bias stress. Maikap *et al.* [89] investigated the charge storage characteristics of atomic layer deposited high-*k* HfO₂/TiO₂ multilayers (ten periods, the thickness of high-*k* HfO₂ or TiO₂ film is ~ 0.5 nm for each layer) in *p*-Si/SiO₂/(HfO₂/TiO₂)/Al₂O₃ structure and. Figure 14(a) showed an HRTEM image of high-*k* HfO₂/TiO₂ multilayers after annealing treatment, in which the high-*k* HfO₂/TiO₂ multilayers were fully crystallized while maintaining the layer-by-layer structure. This was clearly shown in Fig. 14(b), which was processed by Gatan “DIGITAL MICROGRAPH” software. Obviously, there is no intermixing between the HfO₂ and TiO₂ films after high temperature annealing treatment of 900 °C for 1 minute in N₂ ambient.

The high-*k* HfO₂/TiO₂ multilayers in *p*-Si/SiO₂/(HfO₂/TiO₂)/Al₂O₃/aluminum memory capacitors exhibit a memory window of ~ 5 V at gate voltage of ± 5 V due to exiting much quantum wells in the multilayered structure.

5. CONCLUSIONS AND PERSPECTIVE

For conventional floating gate-type nonvolatile semiconductor memories, the challenge is to achieve reliable, low-power, low-voltage performance with the further scaling of device size. Therefore, new flash NVSM technology will be required to overcome these issues. As the promising candidates to replace the conventional floating gate nonvolatile semiconductors memory, SONOS-type memory devices have been investigated widely in the past several years. However, the operating speed and date retention characteristics are bottlenecks for SONOS-type memory devices. Employing high-*k* dielectrics as the charge trapping layer, tunneling layer and blocking layer in these devices is a predominant approach to realize a trade-off between the operating speed and the date retention time. It is found that the single metal oxide (e.g., HfO₂ and ZrO₂) are promising alternative to replace the conventional Si₃N₄. Using rare earth metal oxide as charge trapping layer, such as Y₂O₃, also can improve the memory characteristics. Doping Al₂O₃ into HfO₂ forming binary oxide can obtain a trade-off between operating speed and date retention time. Lee *et al.* [62] proposed a novel SiO₂/SiN/Al₂O₃ structure, in which the conventional blocking layer of SiO₂ was replaced by Al₂O₃. By using blocking materials with higher dielectric constant than the tunneling layer, the electric fields across tunneling layer (E_{TL}) was enhanced and the electric fields across blocking layer (E_{BL}) was suppressed simultaneously. This memory structure has fast operating speed *via* Fowler-Nordheim tunneling mechanism and allows for a thicker tunneling layer over 3 nm. At present, most researches are focused on SONOS-type memories based on this type structure. Multilayered structures, including multilayered tunneling layers or charge trapping layers, are also a promising approach to improve the memory characteristics.

As the development of nonvolatile semiconductor memory technology, the high-*k* dielectrics will replace the conventional Si₃N₄ as the charge trapping layer to obtain higher trap density

and small leakage current. Al_2O_3 is typical blocking material in SONOS structure because of high barrier height and feasible permittivity (~ 9). In the short term, Al_2O_3 as the blocking layer can satisfy the requirements. However, in the long run, employing high- k blocking dielectrics, which have larger permittivity than Al_2O_3 , will be required for further scaling of the thickness. When the thickness of SiO_2 approaches to 2 nm, the leakage current become formidable. Since, in order to realize trade-off between data retention time and operating speed, using high- k dielectrics or stacked structures as the tunneling is necessary.

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