Filed Programmable Logic Control and Test Pattern Generation for IoT Multiple Object switch Control

Kim Eung-Ju[1*], Jung Ji-Hak[2]
[1*]Professor, Dept. of Semiconductor Design, Semiconductor Convergence Campus of Korea Polytechnics
[2]Professor, Dept. of Semiconductor & Display, Asan Campus of Korea Polytechnics

사물인터넷 환경에서 다중 객체 스위치 제어를 위한 프로그래밍 가능한 로직제어 및 테스트 패턴 형성

김응주[1*], 정지학[2]
[1*]한국폴리텍대학 반도체융합캠퍼스 반도체설계과 교수
[2]한국폴리텍대학 아산캠퍼스 반도체디스플레이과 교수

Abstract Multi-Channel Switch ICs for IoT have integrated several solid state structure low ON-resistance bi-directional relay MOS switches with level shifter to drive high voltage and they should be independently controlled by external serialized logic control. These devices are designed for using in applications requiring high-voltage switching control by low-voltage control signals, such as medical ultra-sound imaging, ink-jet printer control, bare board open/short and leakage test system using Kelvin 4-terminal measurement method. This paper describes implementation of analog switch control block and its verification using Field programmable Gate Array (FPGA) test pattern generation. Each block has been implemented using Verilog hardware description language then simulated by Modelsim and prototyped in a FPGA board. Compare to conventional IC, The proposed architecture can be applied to fields where multiple entities need to be controlled simultaneously in the IoT environment and the proposed pattern generation method can be applied to test similar types of ICs.

Key Words : Multi-Channel switch IC, IoT, ON-resistance, shift register, Serialized logic, latch, FPGA

요 약 사물인터넷 환경에서 다중 객체의 스위치 제어는 고전압을 구동하기 위해 레벨 시프터가 있는 여러 솔리드 스테이트 구조로써 낮은 ON 저항과 양방향 릴레이 MOS 스위치를 통합했으며 외부 직렬 논리 제어에 의해 독립적으로 제어되어야 한다. 이 장치는 의료용 초음파 이미지 시스템, 잉크젯 프린터 제어 등의 IoT 기기뿐만 아니라, 켈빈 4 단자 측정을 사용한 PCB 개방 / 단락 및 누출 테스트 시스템과 같은 저전압 제어 신호에 의한 고전압 스위칭 제어가 필요한 응용 제품에 사용하도록 설계되었다. 이 논문에서는 FPGA (Field Programmable Gate Array) 테스트 패턴 생성을 사용한 아날로그 스위치 제어 블록의 구현 및 검증에 대하여 고찰하였다. 각 블록은 Verilog 하드웨어 설명 언어를 사용하여 구현된 후 Modelsim에 의해 시뮬레이션 되고 FPGA 보드에서 프로토타입화 되어 적용되었다. 제안된 아키텍처는 IoT 환경에서 여러개의 개체들을 동시에 제어하여야 하는 분야에 적용할 수 있으며 유사 형태의 IC를 테스트하기 위해 제안된 패턴 생성 방법을 적용할 수 있다.

주제어 : 다중객체, 스위치 제어, 온저항, 쉬프트 레지스터, 직렬화 로직, 래치, FPGA

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*교신저자 : 김응주(keungju@kopo.ac.kr)
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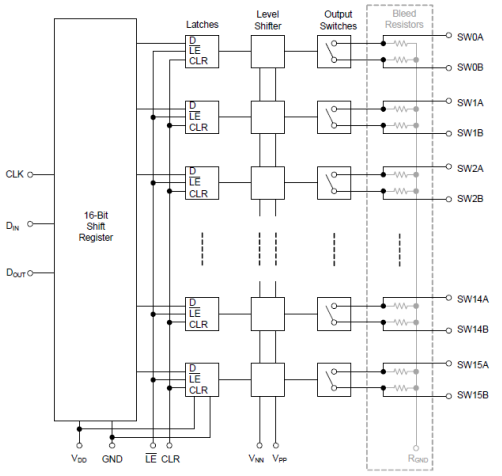
1. Introduction

When configuring a IoT system with multiple switches, such as ultra-sound imaging system, individual discrete analog switches or mechanical relay were used in the past [1-3]. But with the development of semiconductor technology, more than a dozen switches can be integrated into a single IC [4], But with the development of semiconductor technology, more than a dozen switches can be integrated into a single IC [5-7], thousands of switches are now able to efficiently configure Printed Circuit Board (PCB) electrical inspection systems that require them [8]. In an IC in which dozens of switches are integrated, a control input port corresponding to the number of switches is required for individual switch control [9-11]. Usually, ICs are limited in the number of pins that can be used depending on the size of the IC [12-13]. To save the number of individual switch control pin, serializer and deserializer (SerDes) schemes are widely used in input and output IC port and backplane application to compensate for limited input/output [14]. These blocks convert data between serial data and parallel interfaces in each direction [15]. The primary use of a SerDes is to provide data transmission over a single/differential line in order to minimize the number of I/O pins and interconnects. SerDes operation needs data signal with synchronized clock signal [16]. In this paper, we describe a SerDes structure that can reset the switch initial state faster than existing commercial products, and how to design test pattern vectors to test the proposed structure.

2. Multi-Channel Switch IC Operation

2.1 Structures

[Fig. 1] shows a multiple switch IC structure. In this structure, it is necessary to input N bits of serial data and clock in order to initialize the latch state connected to each switch[17]. [Fig. 2] shows conventional 8-bits switch ICs logic operation truth's table. In this table, each switch operates depending on data signal. 8-bits shift register converts serialized DATA to parallel 8-bits data to control each switch using 8-bits synchronized clock signal. The 'DOUT' pin can be used for multi IC connection such as daisy chain connection [18].



[Fig. 1] Multi-Channel Switch IC Structure

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	Hold previous state							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

[Fig. 2] Multi-Channel Switch IC Truth's Table

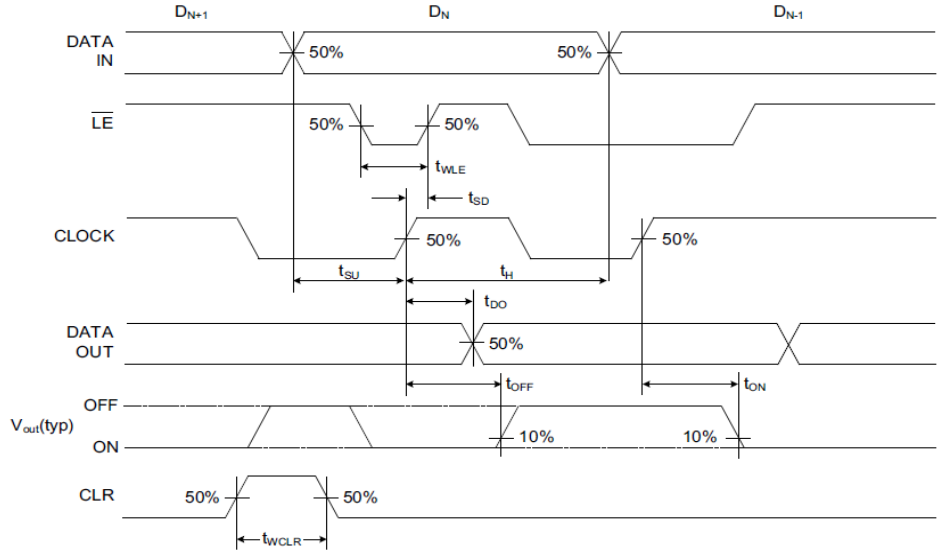
It is composed by connecting several ICs in series and transferring the signals input to the first IC to the connected ICs. The 'DOUT' pin also can be useful to check deserialize conversion correctly. Data is clocked in during the rising edge of the clock. Using High-Voltage CMOS technology, this device combines high-voltage,

bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals. The level shifter block converts the logic level signal into a voltage that can drive the analog switch and must be designed so that the drive current of the drive signal does not flow into the switch. Depending on the state of the LE, the previous switch state can be maintained regardless of the input data.

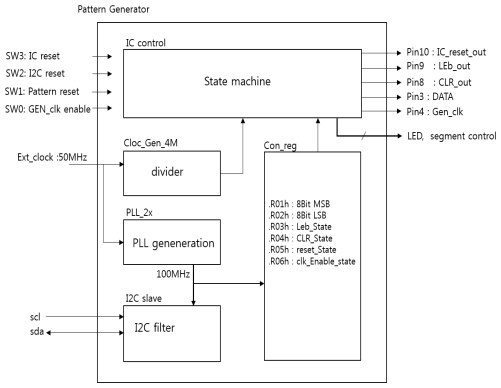
The CLR signal turns off the output of the entire latch. Therefore, the shift register still contains the old data. When the CLR is turned on, the switch operates according to the previous data. In this configuration, each flip-flop is edge triggered. All flip-flops operate at the given clock frequency. Each input bit makes its way down to the output after N clock cycles, leading to parallel output. In cases where the parallel outputs should not change during the serial loading process, it is desirable to use a latched or buffered output. In a latched shift register the serial data is first loaded into an internal buffer register, then upon receipt of a load signal the state of the buffer register is copied into a set of output registers. In general, the practical application of the serial-in/parallel-out shift register is to convert data from serial format on a single wire to parallel format on multiple wires. Therefore, in order to set the shift register to zero state, the conventional IC needs to input serial zero data, so serial data corresponding to the number of switches must be inputted to initialize the entire switch.

2.2 Logic control Implementation

As an example of typical timing diagram of [Fig. 2] for 8-bits multi-channel switch IC can be implemented as shown in the [Fig. 3]. Five input pins are available for switch IC control logic. CLK, Din, CLR, LE. The state of switch (Din) in first loaded into a serial to parallel converter with CLK signal. Whenever the clock signal is input, the data is transferred in sequence to the next register by concatenation operation. At the end of the clock, each data is input to the latch connected in parallel. Additional always statement is used for LEb and CLR latch output control.



[Fig. 3] Logic Input Typical Timing Diagram

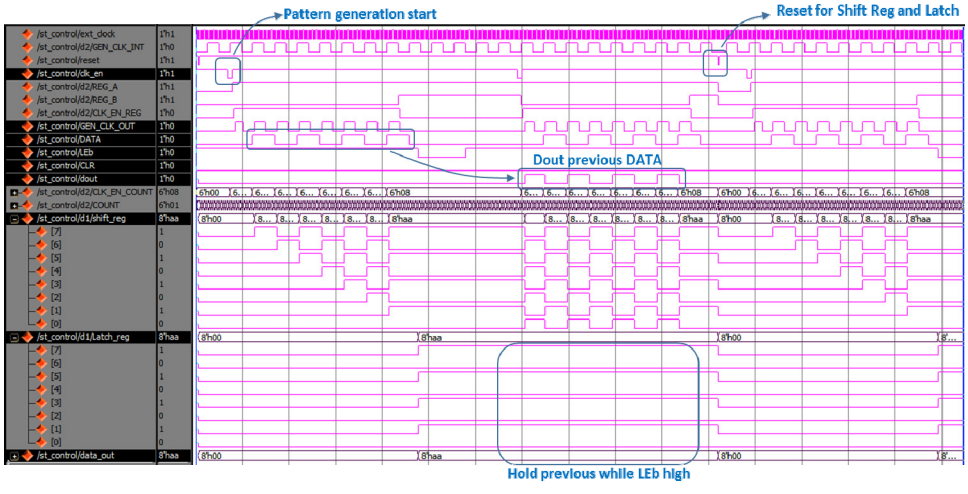


[Fig. 4] Proposed Pattern generation block structure

3. Field Programming Test Pattern Generation

[Fig. 4] shows proposed serialized pattern generation block to generate switch IC input signals. This block interfaces with I2C interface. The state and data of the control signal are stored at [Con_reg]. Each register is made up of 8-bits, and I2C Master and the slave are used for the same address. This block interface with PC by I2C using scl and sda pin. Address of DATA register, LEb, CLR, reset state is also defined in MFC (Microsoft Founded Class) based control program. Using read and write function in control program, control register can be controlled by external interface. This allows several binary devices to be controlled using only two or three pins, but slower than parallel I/O. The 50MHz clock is used as a clock for pattern formation and IC operation by the frequency divider circuit, and it is multiplied by the PLL function of FPGA for I2C.

[Fig. 5] shows the operation of Pattern generation state machine waveform. 8-bits clock synchronized serialized 'DATA' signals are started by pattern generation signal. To make 8-bits clock signal from continuous external clock, The' GEN_clk_EN' signal can be generated a start signal from a button on the FPGA or from a PC. The Flag register 'REG_A' and 'REG_B' are used to indicate the start and end points. Whenever the 'GEN_clk_EN' signal is input, the flag register 'REG_A' is set to the high state. When the internal clock is counted by the number of clocks required for the switch IC to match the IC operation speed, the 'REG_B' flag register indicating the end of the clock is set to high state. In order to make the clock synchronized with the data by the serial data transmission start



[Fig. 5] Simulation Waveform of Pattern Generation

signal from the continuous clock, we make 'CLK_EN_REG' by XOR operation from 'REG_A' and 'REG_B.'. Finally, AND operation of 'CLK_EN_REG' and continuous external clock to make generated clock 'GEN_CLK_OUT' synchronized with DATA. It synchronizes with 'GEN_CLK_OUT' and outputs the DATA signal in synchronization with the stored switch setting bits. The proposed architecture has been verified with 8bits structures. The shift register state changes according to the input data, but the latch register output maintains the previous state when high according to the state of Leb, and outputs the shift register value only when it is low state.

4. Verification

The DE2 Altera FPGA platform was used to verify the proposed pattern generation structure. The test pattern is configured so that the switch selection, reset function and start signal of the test pattern are set in the PC and transmitted to the FPGA by I2C, and the [DOUT] signal is read again to check whether the switch is set properly.

5. Conclusion

In this paper, multi-channel switch ICs shift register with latch control block and field programming pattern generation are proposed. By using additional control bit can reduce all switch sequence time. The proposed scheme is used as a model of IoT test vector program of the back-end test equipment for testing the mass product and can be used for simple automation testing at the initial stage of platform development using FPGA platform.

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김 응 주(Kim Eung-Ju) [종신회원]

- 2011년 2월 : 고려대학교 전자공학과(공학박사)
- 2002년 2월 ~ 2016년 7월 : 삼성전기 중앙연구소 책임 연구원
- 2016년 8월 ~ 현재 : 한국 폴리텍대학 반도체융합캠퍼스 반도체설계과 교수

〈관심분야〉
사물인터넷, 반도체설계, 반도체 장비

정 지 학(Jung Ji-Hak) [종신회원]

- 2006년 8월 : 한양대학교 전자통신전파 공학과 (공학박사)
- 2006년 9월 ~ 2015년 12월 : 삼성전자 S-LSI 수석연구원
- 2015년 12월 ~ 현재 : 한국 폴리텍대학 아산캠퍼스 반도체디스플레이학과 교수

〈관심분야〉
사물인터넷, 반도체 설계, 반도체 소자