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Study on Thermal Analysis for Optimization LED Driver ICs

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This research was analyzed thermal characteristics that was appointed disadvantage when smart LED driver ICs was packaged and we applied extracted thermal characteristics for optimal layout design. We confirmed reliability of smart LED driver ICs package without additional heat sink. If the package is not heat sink, we are possible to minimize package. For extracting thermal loss due to overshoot current, we increased driver current by two and three times. As a result of experiment, we obtained 22 mW and 49.5 mW thermal loss. And we obtained optimal data of 350 mA driver current. It is important to distance between power MOSFET and driver ICs. If the distance was increased, the temperature of package was decreased. And so we obtained optimal data of 3.7 mm distance between power MOSFET and driver ICs. Finally, we fabricated real package and we analyzed the electrical characteristics. We obtained constant 35 V output voltage and 80% efficiency.

Keywords: LED driver, Chip on chip technology, Thermal characteristics, Power loss, Power MOSFET

1. INTRODUCTION

The rapid development of the LED industry since the early 2000s has driven products using LED light sources into global markets for diverse products like automobiles, ships, displays, agricultural, and medical equipment.

LED power supply units (PSUs) have moved from using typical SMPS (switch mode power supply) technology to the use of integrated circuits (ICs). This has driven leading global semiconductor companies to develop control ICs for different kinds of LED PSUs in diverse and expanding markets. These combined factors have driven down the cost down of PSUs to secure more market share, and have increased demand for miniaturization and simplification of the components used for such PSUs [4,5].

Dedicated driver ICs and corresponding standard power metal-oxide-semiconductor field efftect transistors (MOSFETs) had been separately packaged to construct PSUs. With the development of the 700 V class BCDMOS process, integrating a driver IC circuit and power MOSFET on one chip has enabled miniaturization and simplification of PSUs. Many companies striving to develop and release these products to market encounter problems with stabilizing process related technologies. One of these is the technical problem of 'flick' or 'heat up' occurring when integrating on one chip.

In this study, a novel chip-on-chip technology is presented for integrating drive IC and power MOSFET chips in one smaller package. The characteristics of the realized chip are also examined.

2. METHOD OF EXPERIMENT

Figure 1 shows the structure of the conventional 2 chips on

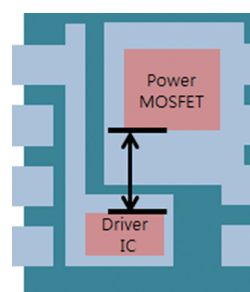

Fig. 1. The structure of conventional 2 chips on 1 package.

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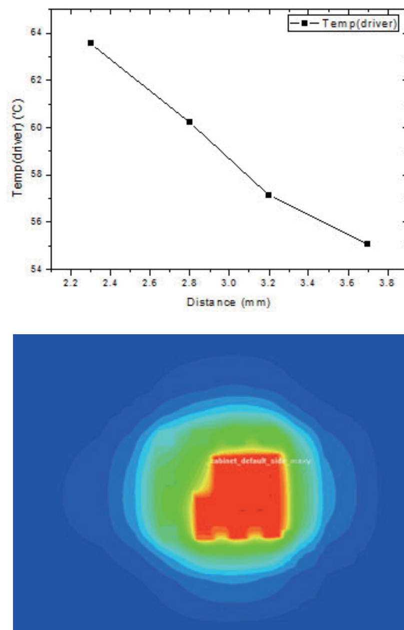

Fig. 2. Thermal characteristics of conventional 2 chips on 1 package according to the distance between power MOSFET and driver ICs.

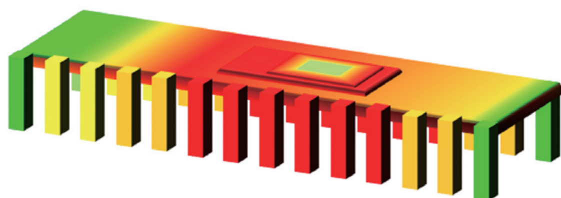

Fig. 3. The proposed structure of chip on chip.

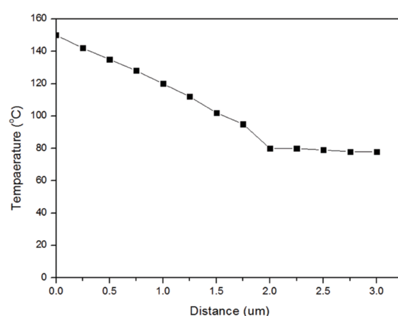

Fig. 4. Thermal characteristics of the chip on chip package according to distance between power MOSFET and driver ICs.

1 package. The prototype of this structure was fabricated as is shown in Fig. 1, and the resulting thermal characteristics of the fabricated prototype were examined. Figure 2 shows the thermal characteristics of the package represented in Fig. 1 where the measured temperature reached 55.06℃ with a maximum distance of 3.7 mm between the MOSFET and driver IC. The red region is high temperature and the blue region is low temperature.

Figure 3 shows the structure of chip-on-chip with the driver IC placed on the power MOSFET package. An experimental simulation was carried out to examine the thermal characteristics of the chip-on-chip package. The results are shown in Fig. 4, where the temperature dropped below 100℃ at the gap point of 1.75 μm.

As in Fig. 2, the red region is high temperature and the green region is low temperature. Additional testing was done with the spacing extended beyond 2 μm. However, the incremental effects were extremely insignificant. The optimal result was attained with a 2 μm gap between the two chips.

3. RESULTS AND DISCUSSION

3.1 Determining the soldering material

Conventional soldering requires direct contact between the bottom electrode and the power semiconductor lead frame using conductive soldering materials. Table 1 summarizes the characteristics of silica as a conventional soldering material. However, using a conductive soldering material for the chip-on-chip technology could affect the mutual operation of the integrated chips. Therefore, proper insulation between the chips is required. After evaluating other soldering materials for fabricating the chip-on-chip package, SiO_2 was selected for its strong insulating properties and used as the soldering material.

Table 1. Characteristics of silica solder material

Color	Black
Gelation time @175℃, sec	20
Spiral flow @175℃, cm	75
Specific gravity, g/cm^3	2.04
Class transition temperature, ℃	165
Thermal expansion α_1, 10^{-6}/℃	26
Thermal expansion α_2, 10^{-6}/℃	73
Flexural strength, Mpa	140
Flexural modulus, Gpa	16
Mold shrinkage, %	0.25
Water absorption, %	0.30
PH	6.0
Electrical conductivity, μs/cm	32
Extracted Na^+, mg/L	3
Extracted CT, mg/L	20
Flammability @UL-94	V-0
Thermal conductivity, W/m-K	1.45

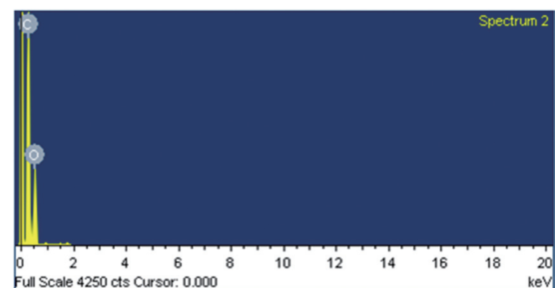

Fig. 5. The extracted data of selected solder material.

3.2 Leadless packaging technology

Complete embodiment of gate driver functions requires a package with a minimum of 12 pins. Using a leadless package, such as shown in Fig. 6, cannot fully utilize the gate driver ICs since it is limited to 10 pins. Therefore, applying a leadless package made exclusively for power semiconductors would be very difficult. Also, general leadless packages are restricted to a maximum thickness of 0.75 mm. If the chip-on-chip technology considered in this study was applied, the 0.83 mm thickness (MOSFET: 0.35 mm, IC: 0.28

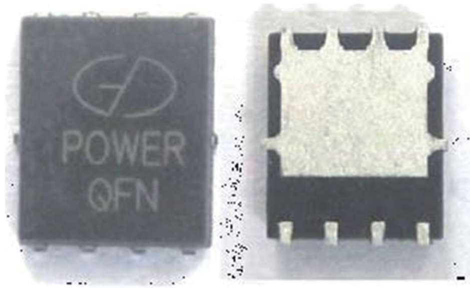

Fig. 6. The conventional power chip package (10pin).

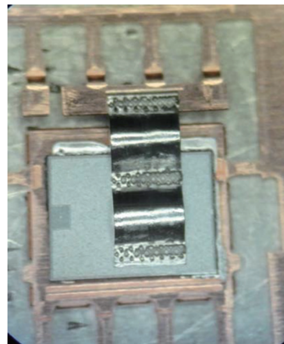

Fig. 7. The conventional structure of connected leadless package.

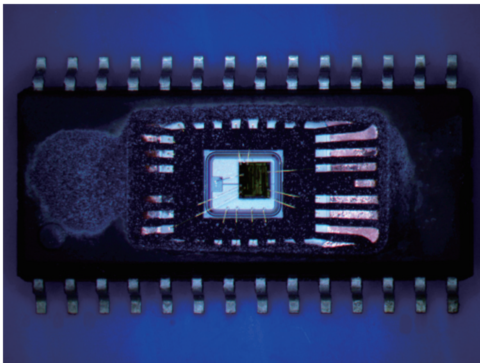

Fig. 8. The proposed chip on chip leadless package.

mm, lead frame: 0.2 mm (where, the thickness of wire bonding and soldering are not taken into account)) exceeds the available thickness.

Therefore, the 'Semi-Leadless' 28-SOP-PKG package was selected. It accommodates the package thickness and allows full use of the gate driver ICs. The package layout of the second prototype is shown in Fig. 6.

Figure 7 shows the internal connection structure of the conventional leadless package, and Fig. 8 shows the internal connection structure of the newly presented chip-on-chip.

3.3 Discussion and results

In the analysis of the thermal characteristics thereof, the temperature increase less than 2℃ in the package under normal temperature was identified and thereby, the resulting reliability of the package requiring no additional heat sink was identified. The level of driving current was increased twice and thrice to derive the thermal loss owing to overshoot current and, the results of thermal loss obtained thereof were 22 mW and 49.5 mW respectively. These values were comparatively stable ones and, by obtaining the optimal value of temperature increase, the driving current of the value of 350 mA was attained.

Besides, as the distance between power MOSFET and driver ICs is a critical factor affecting the temperature increase of the package, the experimental results also rendered the trend of the temperature of package decreased in accordance with the increase of the distance and, the distance of 3.7 mm was derived as the optimal value.

Finally, with the package fabricated by taking the thermal characteristics into account, the output voltage V_out of 32 V was obtained that secured the output level stable against the voltage variation with the output of the I_Out and P_Out which were remaining within the range of ±1 that consequently realized the efficiency over the level of 80%.

4. CONCLUSION

This research was analyzed thermal characteristics that was appointed disadvantage when smart LED driver ICs was packaged and we applied extracted thermal characteristics for optimal layout design. We confirmed reliability of smart LED driver ICs package without additional heat sink. If the package is not heat sink, we are possible to minimize package. For extracting thermal loss due to overshoot current, we increased driver current by two and three times. As a result of experiment, we obtained 22 mW and 49.5 mW thermal loss. And we obtained optimal data of 350 mA driver current. It is important to distance between power MOSFET and driver ICs. If the distance was increased, the temperature of package was decreased. And so we obtained optimal data of 3.7 mm distance between power MOSFET and driver ICs. Finally, we fabricated real package and we analyzed the electrical characteristics. We obtained constant 35 V output voltage and 80% efficiency.

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