An Interleaved Five-level Boost Converter with Voltage-Balance Control

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Abstract

This paper proposes an interleaved five-level boost converter based on a switched-capacitor network. The operating principle of the converter under the CCM mode is analyzed. A high voltage gain, low component stress, small input current ripple, and self-balancing function for the capacitor voltages in the switched-capacitor networks are achieved. In addition, a three-loop control strategy including an outer voltage loop, an inner current loop and a voltage-balance loop has been researched to achieve good performances and voltage-balance effect. An experimental study has been done to verify the correctness and feasibility of the proposed converter and control strategy.

Key words: Five-level, boost, Switched-capacitor, Three-loop, Voltage-balance

I. INTRODUCTION

It is well known that two-stage two-level energy conversion systems composed of a two-level dc-dc converter and a two-level dc-ac inverter, as shown in Fig. 1, are usually utilized in low-voltage applications of less than 1kV. When working on medium-voltage applications with 2.4kV or 3.3kV and megawatt capacity, the two-stage system may not be competent [1]-[3].

Over the past three years, a two-stage multilevel energy conversion system with a novel control method has been developed for wind power generation systems, which output medium-voltage levels [4]-[7]. As shown in Fig. 2, the two-stage multilevel energy conversion system is composed of a multilevel dc-dc converter and a multilevel dc-ac inverter. It can also be seen that they share the same dc link capacitors. Owing to the multilevel structure, the system can operate at relatively low switching frequencies and use fast low voltage devices. More importantly, the dc link capacitors can be controlled by the former multilevel dc-dc converter instead of the latter multilevel inverter, which simplifies the control scheme for the latter multilevel inverter. To achieve a small size and a high power density, non-isolated multilevel dc-dc converters are better than isolated multilevel dc-dc converters. In addition, the presence of a high voltage gain and a small ripple are both welcome.

The authors of [8] proposed a multilevel boost converter (MBC) based on voltage multipliers, which has a high voltage gain and a self-balance function for capacitor voltages. In addition, this function can be advantageous for balancing the dc link capacitor voltages as shown in Fig. 2 [9, 10]. An interleaved multilevel boost converter based on a MBC is proposed to reduce input current ripple [11]. However, more components are necessary, which makes this a poor choice. New four-level and a five-level boost converters together with their corresponding modulation strategies have been proposed in [12]-[14]. However, the voltage gains of these converters are not high. Another possible solution is the application of a diode-capacitor voltage multiplier on classical non-isolated dc-dc converters [15]-[17]. These converters exhibit high voltage gains and low voltage stress. However, the input current ripple is very high since no interleaved schemes are adopted. Recently, switched-capacitor techniques have been researched and applied to medium-voltage and high-power dc-dc converters, and good performance has been achieved [18]-[20].

In the paper, a five-level boost converter based on a switched-capacitor technique is proposed. This paper is organized as follows: Section II introduces the operation
signals, which are phase-shift 180 degrees with the same duty cycle. A three-loop control strategy including an outer voltage loop, an inner current loop and a voltage-balance loop, is proposed to solve the neutral-point potential imbalance issue in Section III. Experimental verifications are presented in Section IV. Finally, some conclusion are drawn at the last section.

II. THE PROPOSED CONVERTER

The three-level boost converter shown in Fig. 3(a) has been widely used in renewable generation applications. However, it cannot be used in high voltage applications since its output level is limited to three. The five-level boost converter shown in Fig. 3(b) was proposed in [14]. Since it can output five voltage levels, the voltage stresses across the components are smaller than those of the three-level boost converter. However, both converters show low voltage gains and the five-level boost converter has many switches with a complex voltage-balance control strategy since four capacitor voltages are sampled and controlled.

According to the above analysis, a five-level boost converter is proposed based on the switched-capacitor network in Fig. 4. The two switched-capacitor networks are labelled as switched-capacitor I and switched-capacitor II. The switches $S_1$ and $S_2$ are controlled by two different drive signals, which are phase-shift 180 degrees with the same duty cycle. Equivalent circuits of the converter are presented in Fig. 5 and typical waveforms are given in Fig. 6. To ensure balanced capacitor voltages, all of the capacitors have the same capacitance and two switches. In addition, all of the diodes have the same parameters.

Stage I: when $S_1$ and $S_2$ are both turned on, $D_2$ and $D_3$ are forward biased while $D_1$, $D_4$ and $D_5$ are reverse biased, as shown in Fig. 5(a). During this period, the inductor $L$ is charged by the input source $U_{in}$. If $U_{C1}$ is smaller than $U_{C4}$, then $U_{C4}$ clamps $U_{C1}$ through $S_1$ and $D_2$. If $U_{C2}$ is smaller than $U_{C5}$, then $U_{C5}$ clamps $U_{C2}$ through $S_2$ and $D_3$. Therefore, the following expressions can be given:

$$u_L = U_{in} \quad (1)$$
$$U_{C1} = U_{C4} \quad (2)$$
$$U_{C2} = U_{C5} \quad (3)$$

Stage II: when $S_1$ is turned on while $S_2$ is turned off, $D_2$, $D_3$...
When the duty cycle \( d \) is bigger than 0.5, the converter operates in the stages I, II, I and III; and when \( d \) is smaller than 0.5, it operates in the stages IV, II, IV and III. No matter what \( d \) is, the same output results can be achieved according to (1)-(12):

\[
U_o = \frac{2}{1-d} U_i \quad (13)
\]

\[
I_L = \frac{2}{1-d} I_o \quad (14)
\]

In addition, all of the capacitor voltages can be achieved:

\[
U_{C1} = U_{C2} = U_{C3} = U_{C4} = U_{C5} = U_{C6} = \frac{1}{4} U_o \quad (15)
\]

### III. VOLTAGE-BALANCE CONTROL

As analyzed in Section II, the proposed converter has a self-balance function for some of the capacitor voltages due to the switched-capacitor technique. \( U_{C1} \), \( U_{C3} \) and \( U_{C4} \) are self-balanced with one uniform voltage level, while \( U_{C2} \), \( U_{C5} \) and \( U_{C6} \) are self-balanced with another uniform voltage level. To make the two different voltage levels balanced, a three-loop control strategy including an outer voltage loop, an inner current loop and a voltage-balance loop is proposed, as shown in Fig. 7.

The outer voltage loop is adopted to keep the output voltage stable and the inner current loop is adopted to improve the dynamic performance of the converter. More importantly, the voltage-balance loop is used to make the two different voltage levels balanced. That is to say, all of the capacitor voltages can be equalized by the voltage-balance loop. It should be noted that the two carrier signals \( C_{a1} \) and \( C_{a2} \) in Fig. 7 are phase-shifted 180 degrees to implement the interleaved scheme for \( S_1 \) and \( S_2 \).

\( U_o^* \) and \( I_o^* \) represents the reference output voltage and the reference inductor current, respectively. The goal of the outer voltage loop and the inner current loop is to get the duty cycle \( d_i \) of \( S_1 \). In addition, a difference duty cycle \( \Delta d \) is achieved through the PI controller by a difference voltage \( \Delta U \). Then, the duty cycle \( d_2 \) of \( S_2 \) can be easily obtained as follows:

\[
d_2 = d_1 + \Delta d \quad (16)
\]

Two definitions are given as follows:

\[
U_i = U_{C3} + U_{C4} \quad (17)
\]

\[
U_2 = U_{C5} + U_{C6} \quad (18)
\]

Therefore, the voltage-balance process is: when \( U_i \) is bigger than \( U_2 \), \( \Delta d \) becomes negative, which makes \( d_2 \) a little smaller than \( d_1 \). That is to say, the turn-on time of \( S_1 \) is a little larger than that of \( S_2 \), which makes the charging time of \( C_3 \) a little larger than that of \( C_4 \). Thus, \( U_2 \) increases while \( U_i \) decreases. Finally \( U_2 \) is equal to \( U_i \) after several switching periods. In addition, when \( U_i \) is smaller than \( U_2 \), the same result can be achieved based on a similar voltage-balance process. Since the output capacitor voltages are balanced, the
proposed five-level boost converter is a good choice to connect with five-level or three-level diode-clamped inverters.

IV. PERFORMANCE ANALYSIS

A. Performance

According to (13)-(15), it is clear that a high voltage gain and small capacitor voltages can be achieved with the proposed converter. In addition, it can be seen that the voltage stresses across all of the switches and diodes are equal to the capacitor voltages, which are just a quarter of the output voltage. Additionally, according to (2), (3), (6) and (9), it can be concluded that \( C_1, C_3 \) and \( C_4 \) are balanced with a uniform voltage level and that \( C_2, C_5 \) and \( C_6 \) are balanced with another uniform voltage level. The balanced process is called the self-balance function. In addition, the proposed converter is similar to a three-level boost converter. Thus, \( U_C4 \) is commonly not equal to \( U_C5 \), which makes the two uniform voltage levels different in practical applications. It behaves as the neutral-point potential imbalance issue. However, the two uniform voltage levels can be equalized with a simple voltage-balance loop, which has been presented in Section III.

Additionally, the inductor current ripple is:

\[
\Delta i_L = \begin{cases} 
\frac{U_{in} 2d - 1}{2L} f_s & d > 0.5 \\
\frac{U_{in} d(1-2d)}{2L (1-d) f_s} & d \leq 0.5
\end{cases}
\] (19)

B. Condition for the CCM

The CCM occurs when the average inductor current is bigger than the peak inductor current ripple:

\[
I_s > \frac{\Delta i_L}{2}
\] (20)

The integration of (13), (14) and (19) into (20) yields the following condition for the DCM operation mode when the duty cycle \( d \) is bigger than 0.5:

\[
K > K_{crit}
\] (21)

Where the dimensionless parameter \( K \) is defined as follows:

\[
K = \frac{2Lf_s}{R}
\] (22)

In addition, the coefficient \( K_{crit} \) can be expressed as follows:

\[
K_{crit} = \begin{cases} 
\frac{(2d-1)(1-d)^2}{8} & d > 0.5 \\
\frac{d(1-d)(2d-1)}{8} & d \leq 0.5
\end{cases}
\] (23)

When \( d \) is bigger than 0.5, the maximum value of \( K_{crit} \) is 0.0046 at \( d=2/3 \). When \( d \) is smaller than 0.5, the maximum value of \( K_{crit} \) is 0.012 at \( d=0.211 \). On the whole, the maximum value of \( K_{crit} \) for the proposed converter should be:

\[
(K_{crit})_{max} = 0.012
\] (24)

Then, if it is necessary to let the proposed converter operate in the CCM mode, the result will be achieved based on (21) and (24) as follows:

\[
2Lf_s > 0.012
\] (25)

(25) can be further simplified as:

\[
L > \frac{0.006R}{f_s}
\] (26)

(26) is an important guide to make the converter operate under the CCM mode.

C. Comparative Analysis

The proposed five-level boost converter in Fig. 4 is similar to the five-level boost converter in Fig. 3(b). A comparative analysis between the two converters is listed in Table I. In this table, \( G \) represents the voltage gain and \( U_{vp} \) represents the voltage stress.

<table>
<thead>
<tr>
<th>Topology</th>
<th>( L )</th>
<th>( S )</th>
<th>( D )</th>
<th>( C )</th>
<th>( G )</th>
<th>( U_{vp} )</th>
<th>Ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 3(b)</td>
<td>1</td>
<td>4</td>
<td>4</td>
<td>1/(1-d)</td>
<td>( U_o/4 )</td>
<td>Small</td>
<td></td>
</tr>
<tr>
<td>Fig. 4</td>
<td>1</td>
<td>2</td>
<td>6</td>
<td>2/(1-d)</td>
<td>( U_o/4 )</td>
<td>Small</td>
<td></td>
</tr>
</tbody>
</table>

\[
K_{crit} = \begin{cases} 
\frac{(2d-1)(1-d)^2}{8} & d > 0.5 \\
\frac{d(1-d)(2d-1)}{8} & d \leq 0.5
\end{cases}
\] (23)

When \( d \) is bigger than 0.5, the maximum value of \( K_{crit} \) is 0.0046 at \( d=2/3 \). When \( d \) is smaller than 0.5, the maximum value of \( K_{crit} \) is 0.012 at \( d=0.211 \). On the whole, the maximum value of \( K_{crit} \) for the proposed converter should be:

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\[
2Lf_s > 0.012
\] (25)

(25) can be further simplified as:

\[
L > \frac{0.006R}{f_s}
\] (26)

(26) is an important guide to make the converter operate under the CCM mode.

In addition, the two switched-capacitor networks in Fig. 4 have the self-balance function for the capacitor voltages, only two capacitor voltages \( U_{C1} \) and \( U_{C2} \) should be sampled and controlled. On the whole, the neutral-point potential control strategy is easy to implement. However, for the five-level boost converter in Fig. 3(b), it is difficult to realize the neutral-point potential control strategy because four capacitor voltages \( U_{C3}, U_{C4}, U_{C5} \) and \( U_{C6} \) need to be sampled and controlled. In addition, when the capacitances of the four capacitors are different, it is more difficult to make them balanced.
TABLE II
EXPERIMENTAL PARAMETERS

<table>
<thead>
<tr>
<th>Components</th>
<th>Rated Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage $U_{in}$</td>
<td>36V-100V</td>
</tr>
<tr>
<td>Output voltage $U_o$</td>
<td>300V</td>
</tr>
<tr>
<td>Load R</td>
<td>400ohm</td>
</tr>
<tr>
<td>Output power</td>
<td>225W</td>
</tr>
<tr>
<td>Switching frequency $f_s$</td>
<td>20kHz</td>
</tr>
<tr>
<td>Inductor $L$</td>
<td>508μH</td>
</tr>
<tr>
<td>Capacitors $C_1 - C_6$</td>
<td>470uF</td>
</tr>
</tbody>
</table>

V. EXPERIMENTAL VERIFICATION

In the experimental part, a prototype with a small output power, presented in Fig. 8, is built to verify the feasibility of the proposed converter. The experimental parameters are presented in Table II and the experimental study has been done under the CCM mode. According to (26), the inductance of $L$ can be calculated as follows:

$$\frac{L}{f_s} > \frac{0.006R}{f_s} = \frac{0.006 \times 400}{20000} = 120(\mu H)$$ (27)

According to (27), if the inductance of $L$ is bigger than 120μH, the converter operates under the CCM mode. In this paper, the inductance of $L$ is selected to be about 508μH.

Key experimental waveforms of the converter under different input voltages are presented in Fig. 9, including waveforms of the driven signals, inductor current and output voltage. Voltage waveforms for all of the switches and diodes under an input voltage of 36V are presented in Fig. 10. In addition, dynamic experimental waveforms of the converter when the input voltage varies and the output voltage varies are presented in Fig. 11. Furthermore, the voltage-balance results are presented in Fig. 12. Moreover, the conversio efficiency curves of the converter under different input voltages are also given in Fig. 14.

As can be seen from Fig. 9, the output voltage is stable at 300V under different input voltages. The input current is continuous with a small current ripple, and the ripple frequency 40kHz is two times the switching frequency 20kHz. Moreover, when the input voltage is 80V, the duty cycles of $S_1$ and $S_2$ are both about 0.50, which makes the input current ripple nearly equal to zero. This can be verified by Fig. 9(c).

The source terminal of the switches $S_1$ and $S_2$. In addition, $u_{Di}$ ($i=1, 2, 3, 4, 5, 6$) are defined to describe the electric potential difference between the cathode terminal and the anode terminal of the diodes $D_1-D_6$.

It should be noted that $S_1$ and $S_2$ are given to present the drive signals, and $u_{S1}$ and $u_{S2}$ are defined to describe the electric potential difference between the drain terminal and the source terminal of the switches $S_1$ and $S_2$. In addition, $u_{Di}$ ($i=1, 2, 3, 4, 5, 6$) are defined to describe the electric potential difference between the cathode terminal and the anode terminal of the diodes $D_1-D_6$.

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Fig. 10. Voltage waveforms of the switches and diodes under the input voltage 36V: (a) $u_{S1}, u_{D1}, u_{D2}, u_{D3}$; (b) $u_{S2}, u_{D4}, u_{D5}, u_{D6}$; (c) $U_{C1}, U_{C3}, U_{C4}$; (d) $U_{C2}, U_{C5}, U_{C6}$.

The stresses for all of the switches, diodes, and capacitors in the converter are about 75V, which is only a quarter of the output voltage 300V. It should be noted that the six capacitors $C_1$-$C_6$ in the converter have nearly the same capacitor voltage. However, some voltage differences exist due to the voltage drops of the devices.

On the other hand, the converter can still output a stable voltage when the input voltage varies suddenly, as shown in Fig. 11(a). In addition, the input average current varies to make the converter achieve a steady output power. In Fig. 11(b), the output voltage increases and then decreases according to variations of the referring output voltage. In addition, the duty cycles and the average input current change like the output voltage, since the load is invariant. Fig. 12 shows that the capacitor voltages of $C_1, C_2, C_3, C_4, C_5$, and $C_6$ can be nearly equalized with a uniform voltage level when the voltage-balance loop is considered in the closed-loop control strategy. In Fig. 13, when $C_3$ and $C_4$ are changed to 47uF, the voltages of $C_3$ and $C_4$ are about 15V, while the voltages of $C_5$ and $C_6$ are about 135V. However, when the voltage-balance loop is added, they are all balanced with the
same voltage level 75V.

All of these experimental results basically match with the theoretical analysis in section II and III, which demonstrates that the proposed converter is feasible. In addition, it can be seen from Fig.14 that the maximum conversion efficiency of the proposed converter is 89.9% with a 36V input voltage, 92.6% with a 60V input voltage, and 93.8% with both 80V and 100V input voltages. Furthermore, it is not difficult to conclude from Fig.14 that the larger the input voltage is, the larger the conversion efficiency becomes. This is due to the fact that when the input voltage is very low, a very high input current is produced to make the converter achieve a stable output power. However, a high input current increases the losses of the inductor, the switches and the diodes due to the presence of parasitic resistance, forward voltage drops and other non-idealities.

VI. CONCLUSION

This paper introduces a five-level boost converter, which can increase the input voltage to a high voltage level, attain a low component voltage stress, and achieve a small input current ripple. The operating principle of the converter under the CCM mode and the performances are analyzed. A three-loop control strategy has been presented to solve the neutral-point potential imbalance issue. In addition to good stable and dynamic performances, the capacitor voltages can be easily balanced due to the self-balance function of the two switched-capacitor networks and the voltage-balance loop. Finally, experimental results verify the correctness and feasibility of the proposed converter and control strategy.

REFERENCES

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