Full ZVS Load Range Diode Clamped Three-level DC-DC Converter with Secondary Modulation

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Abstract

A new four-primary-switch diode clamped soft switching three-level DC-DC converter (TLDC) with full zero-voltage switching (ZVS) load range and TL secondary voltage waveform is proposed. The operation principle and characteristics of the presented converter are discussed, and experimental results are consistent with theoretical predictions. The improvements of the proposed converter include a simple and compact primary structure, TL secondary rectified voltage waveform, wide load range ZVS for all primary switches, and full output-regulated range with soft switching operation. The proposed converter also has some disadvantages. The VA rating of the transformer is slightly larger than that of conventional TLDCs in variable input and constant output mode. The conduction loss of the primary coil is slightly higher because an air gap is inserted into the magnetic cores of the transformer. Finally, the secondary circuit is slightly complex.

Key words: No circulating current, Reduced filter size, Three-level (TL) DC/DC converter, Zero-voltage switching (ZVS)

I. INTRODUCTION

Three-level DC-DC converters (TLDCs) have become a key issue in power electronics because of the rapidly increasing demand for high-input and high-efficiency isolated DC-DC power supplies [1], [2]. Interest in these devices stems from the research of Pinheiro and Barbi, who first introduced multilevel technology to the DC-DC power conversion field [1]. Five basic TLDCs were discussed and compared in [3], and most existing TLDCs are derived from these five topologies. A zero-voltage and zero-current switching (ZVZCS) TLDC was proposed in [4], in which a flying capacitor is used to assist zero-voltage switching (ZVS) of the leading switches, and an auxiliary secondary current reset circuit is added to assist in the zero-current switching (ZCS) of the lagging switches. Moreover, the converter in [4] can be switched in the phase shift (PS) mode, which makes this topology applicable. Many satisfactory contributions have been made to this topic. New TLDCs that have different useful features are proposed in [5]-[9]. Some good solutions that extend the soft switching load range of the primary switches were provided in [10]-[13]. A full bridge (FB) TLDC for wind turbines in a DC grid was investigated in [14]. Improved control strategies were discussed in [15] and [16]. All the references listed above have made the TLDCs applicable.

However, limitations still exist. In most TLDCs, the secondary rectified voltage is a two-level waveform. Large voltage ripple across the output filter requires a larger output inductor to smoothen the ripple current that flows through it, thereby increasing the overall system volume and slow down possible system dynamic responses [3], [17]-[21]. Furthermore, the input current is discontinuous, thereby requiring a large input filter to confirm the corresponding electromagnetic compatibility standards [3]. Several papers have been published to solve the abovementioned problems. A ZVZCS hybrid FB TLDC was proposed in [17], which can obtain a three-level (TL) secondary rectified voltage waveform before the output filter. In addition, two cutoff diodes are added to minimize the switching loss of the lagging switches [17]. A TL combined DC-DC converter (TLCDC) with six power switches was proposed in [18], which features even voltage stress on the primary devices and TL secondary rectified voltage waveform. The converter in [18] has good soft switching characteristics because it utilizes ZVZCS technology. In [19], an FB TLCDC was proposed,
which can achieve a TL secondary rectified voltage waveform before the LC filter, as well as wide ZVS load range for all primary switches. A TLCDC with no added clamping device was discussed in [20]. To find a new topology with a simple and compact primary circuit, a TLCDC with four switches was proposed in [21], which has the minimum number of the primary switches among all TLCDCs. However, the main disadvantage of this converter is the limited output range with ZVS operation. During some abnormal situations, i.e., startup or overload/short circuit, the converter in [21] can only be switched in the hard switching mode to regulate the output voltage down to zero. Furthermore, the ZVS load range of the lagging switches in [21] is limited because only the energy stored in the leakage inductances can be used. Thus, a new TLDC characterized by a TL secondary rectified voltage waveform, simple and compact primary power circuit, good soft switching characteristics, and wide output range with soft switching operation must be found.

A diode-clamped TLDC with full ZVS load range, TL secondary rectified voltage waveform, and wide output range with soft switching operation is proposed in this paper. This paper is organized as follows: In Section II, the configuration and operation principle of the proposed converter are described. In Section III, important technical issues are discussed. In Section IV, experimental results are presented and discussed. In the last section, the main conclusions are given.

II. CONFIGURATION AND OPERATION PRINCIPLE

A. Configuration

Fig.1 shows the circuit of the proposed converter. The four primary switches are series connected, and the off-state voltage of these switches is clamped by D o1, D o2, C in1, and C in2. C in1 and C in2 are the input capacitors with the same value and share the input voltage evenly during the operation, i.e., \( V_{Cin1} = V_{Cin2} = \frac{V_{in}}{2} \). L lk is the equivalent leakage inductance in the primary side of the transformer. L m is the magnetizing inductance. The turn ratios in the proposed converter are set at \( N_{p1}/N_{s1} = k_1 \) and \( N_{p2}/N_{s2} = k_2 \). S e1 and S e2 are the secondary switches. D o1–D o6 are the rectifier diodes, and the output filter is composed of L o and C o, Ro is the load resistor.

B. Normal Operation

Fig.2 depicts the key waveforms. Twelve operation stages are present during the entire switching cycle, and the operation stages in the first half-switching cycle are illustrated in Fig.3. Before the analysis, some assumptions are set to simplify the explanation: all the components in the topology are ideal; the voltage ripple on C in1 and C in2 can be neglected; \( k_T' = (k_{1T'} + k_{2T'}) / (k_{1T'} + k_{2T'}) \); and the output filter and load are replaced by a constant current source I o. The output capacitance of each primary switch is with the same value and represented as C o in the following equations.

Stage 1 [Fig.3 (a)]: Before t o, the circuit is operated in a steady condition. The primary side powers the load. S 1 and S 2 are on; D o3 and D o6 are conducted; S e2 is also on, but the current that flows through S se2 is zero because D o2 is off. \( V_{BA} = V_{in}/2 \), \( V_{rect} = V_{in}/2k_{T2} \), \( i_p = I_o/k_{T2} \), \( i_{Lk} \) equals the sum of \( i_p \) and \( i_m \), \( i_m \) increases with time linearly, and the slope is

\[
\frac{di_m}{dt} = \frac{V_m}{2L_m}.
\]

Stage 2 [Fig.3 (b), t o–t 1]: At the instant t o, S e2 is turned off at zero-current. Primary side powers the load. \( V_{BA} = V_{in}/2, V_{rect} = V_{in}/2k_{T2}, i_p = I_o/k_{T2}, i_{Lk} \) equals the sum of \( i_p \) and \( i_m \), and \( i_m \) keeps increasing.

Stage 3 [Fig.3 (c), t 1–t 2]: At the instant t 1, S e2 is turned on, D o3 is conducted, and D o6 is off. The primary side powers the load. \( V_{BA} = V_{in}/2, V_{rect} = V_{in}/2k_{T2}, i_p = I_o/k_{T2}, i_{Lk} \) equals the sum of \( i_p \) and \( i_m \), and \( i_m \) linearly increases with time.

Stage 4 [Fig.3 (d), t 2–t 3]: At t 2, S 1 and S 2 are simultaneously turned off at zero voltage because of the existence of C 1 and C 2; \( i_{Lk} \) charges C 1 and C 2 and discharges C 3 and C 4 linearly with time. During this interval, the value of \( i_m \) can be treated as a constant value, which is represented by \( I_m \) in the following equations. The voltage of point B decreases linearly with time before \( V_{rect} \) is zero, and its value is
After freewheeling mode is over, The primary side continuously flows through $S_{se1}$ is zero because $D_{o1}$ is off. After stage 6, and the slope is determined by Eq. (1). The current that $i_{p}$ reaches $-i_{o}/k_{T2}$, the freewheeling mode is over. The primary side continuously powers the load. After $t_{o}$, $v_{BA}=-V_{in}/2$, $v_{rect}=-V_{in}/2k_{T2}$, $i_{p}=-i_{o}/k_{T2}$, $i_{LK}$ equals the sum of $i_{p}$ and $i_{o}$. $i_{LK}$ linearly decreases with time, and the slope is determined by Eq. (1). The current that flows through $S_{se1}$ is zero because $D_{o1}$ is off. After stage 6, the circuit will be operated in the second half-switching cycle. As shown in Fig.3, during normal operation, the current that flows through $D_{o1}$and $D_{o2}$is zero, which means a lower current rating requirement of $D_{o1}$and $D_{o2}$.

Stage 5 [Fig.3 (e), $t_{4}$–$t_{5}$]:
The circuit is maintained in freewheeling mode; $S_{3}$ and $S_{4}$ must be turned on to achieve ZVS.

Stage 6 [Fig.3 (f), $t_{5}$–$t_{6}$]:
The current rating requirement of $D_{cl1}$ and $D_{cl2}$.

\[
v_{BA} = v_{BA} - \frac{V_{m}}{2} - \left[ \frac{i_{o} + i_{m}}{k_{T1}} \right] t.
\]

\[
v_{rec} = v_{BA} \cdot k_{T1}.
\]

\[
v_{rec} = \frac{V_{m}}{2} \cdot \frac{1}{k_{T1}} + \frac{i_{m}}{k_{T1}} t.
\]

\[
v_{rec} = \frac{V_{m}}{2} \cdot \frac{1}{k_{T1}} + \frac{i_{m}}{k_{T1}} t.
\]

When \( v_{rec} \) is zero, the voltage of point B can be calculated by Eqs. (2) and (5), which is $V_{m}/2$. The time of this period is

\[
T_{z2} = \frac{V_{m} \cdot C_{m} \cdot k_{T1}}{2(i_{o} + i_{m} \cdot k_{T1})}.
\]

After $t_{5}$, the circuit will be operated in freewheeling mode. $i_{LK}$ charges $C_{1}$ and $C_{2}$, and discharges $C_{3}$ and $C_{4}$ linearly with time. This stage ends until $V_{C1}=V_{C2}=V_{m}/2$, and $v_{C3} = v_{C4} = 0$.

\[
v_{BA} = v_{BA} - \frac{V_{m}}{2} - \left[ \frac{i_{o} + i_{m}}{k_{T1}} \right] t.
\]

\[
v_{rec} = \frac{V_{m}}{2} - \frac{i_{o} + i_{m}}{k_{T1}} t.
\]

\[
v_{rec} = \frac{V_{m}}{2} - \frac{i_{o} + i_{m}}{k_{T1}} t.
\]

C. Soft Start Operation

Fig. 4 illustrates key waveforms during soft start operation, and the voltage stress on the secondary devices is provided in Table II. During soft start, $S_{se1}$ and $S_{se2}$ are off, and the proposed converter can be treated as a conventional diode-clamped TLDC in [1]. The operating principle for this procedure is not provided here for the sake of simplicity, and detailed information can be found in [1].

III. TECHNICAL ANALYSIS

A. ZVS of Primary Switches

During the operation, the four switches are gated in the complementary mode, and these switches can obtain ZVS down to no-load with a specified peak value of $i_{o}$. $S_{1}$ in Fig.1 is selected as an example. Fig. 3(d) shows the equivalent
TABLE II

<table>
<thead>
<tr>
<th>Power devices</th>
<th>Maximum voltage stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{se1}, S_{se2}$</td>
<td>$V_{in}/2 k_{T1}$</td>
</tr>
<tr>
<td>$D_{o3}, D_{o4}, D_{o5}$ and $D_{o6}$</td>
<td>$V_{in}/2 k_{T2}$</td>
</tr>
<tr>
<td>$D_{o1}$ and $D_{o2}$</td>
<td>$V_{in}/2 k_{T}$</td>
</tr>
</tbody>
</table>

circuit of this procedure. The switching interval can be divided into two sub-stages. In the first sub-stage, $v_{rect}>0$, and the load current can still be used to charge or discharge corresponding capacitors. As proved in Section II, when $v_{rect}=0$, 50% of the final value of the voltage across $C_3$ has been discharged. Thus, only half of the voltage across $C_3$ needs to be charged during the secondary sub-stage. In the secondary sub-stage, $v_{rect}=0$, and the energy stored in the leakage inductance is used to discharge or charge corresponding capacitors. To achieve ZVS, the following equation should be fitted:

$$\sin m 22 V_L \Delta I_m \leq \frac{V_m}{\cos \phi}.$$  \hspace{1cm} (8)

The peak-to-peak value of $I_m$ is

$$\Delta I_m = \frac{V_m T_s}{2 L_m} = 2 I_m.$$  \hspace{1cm} (9)

Thus, $I_m$ is

$$I_m = \frac{V_m T_s}{4 L_m}.$$  \hspace{1cm} (10)

Substituting Equ. (10) into Equ. (8) obtains

$$L_m \leq \frac{3}{4} \frac{T_s}{V_m} \frac{L_k}{C_{os}}.$$  \hspace{1cm} (11)

Therefore, $S_3$ can obtain ZVS down to a zero-load current with a specific value of $L_m$ decided by Equ. (11). Fig 6 shows the required magnetizing inductance versus $C_{os}$, $L_k$, and $T_s$. To obtain a small magnetic inductance, an air gap should be inserted in the magnetic cores. The main disadvantage caused by the added air gap is higher conduction loss of the primary coil compared with that of conventional power transformer with no air gap.

The conduction loss is related to the RMS value of the primary current. Increasing $I_m$ in the proposed converter will add some conduction loss. However, the added conduction loss is much lower than that of a traditional PS controlled DC–DC converter with a larger value of $I_m$. Fig 7 shows the magnetizing current comparison among the proposed converter and the converter in conventional PS controlled DC–DC converter. As shown in Fig. 7(a), the average value of $I_m$ is zero during the half-switching period, and this current is not in phase with the load current. Thus, a larger value of $I_m$ will not cause much added RMS or average absolute value of the primary current and add more conduction loss in the conventional PS controlled DC–DC converter.
The converter should be designed as

\[ k_{T_2} = \frac{V_{\text{inmax}}}{2V_o} \]  

and

\[ \frac{k_{T_1}k_{T_2}}{k_{T_1} + k_{T_2}} = \frac{V_{\text{inmin}}}{2V_o} \]  

As for a converter with 600 to 800 V input and 300 V output (used in the prototype), \( k_{T_2} \) can be decided by Eqn. (12), and the value is 1.33; according to Eqn. (13), \( k_{T_1} = 4.03 \).

During normal operation, the ideal relationship between the output voltage and the input voltage can be achieved by neglecting the effect of the leakage inductance, and \( V_o \) is

\[ V_o = (1 - D) \frac{V_{\text{inmax}}}{2k_{T_2}} + D \left(\frac{V_{\text{in}}}{2k_{T_2}} + \frac{V_{\text{inmin}}}{2k_{T_1}}\right) \]  

where \( D \) is the duty ratio of voltage level \( V_{\text{in}}/2k_{T_1} \), and Eqn. (14) can be further simplified as

\[ V_o = \frac{V_{\text{in}}}{2k_{T_2}} + D \frac{V_{\text{inmin}}}{2k_{T_1}} \]  

During soft start operation, the ideal relationship between output voltage and input voltage is

\[ V_o = D \frac{V_{\text{in}}}{2k_{T_2}} \]  

where \( D \) is the duty ratio of voltage level \( V_{\text{in}}/2k_{T_2} \).

### D. Reduced Output Inductance Value

The reduction of the output inductance with TL secondary rectified voltage waveform has been discussed in several works [17]-[21]. According to these references, if \( V_{\text{inmax}}: V_{\text{inmin}} = 2:1 \), the required output inductance of the converters with TL secondary rectified voltage waveform is approximately one-third that of conventional converters with two-level secondary rectified voltage. Therefore, the volume of the output filter in the proposed converter can be reduced significantly.

### E. Comparison

The proposed converter is compared with conventional diode-clamped TLDC and a TLDC with four primary switches in this part. The circuits of the converters for comparison are provided in Fig.9, and the detailed operation principle about these converters can be found in [1] and [21]. Table III illustrates the component number comparison among these converters, and the current and voltage rating of the primary components is provided in Table IV. Power loss comparison is listed in Table V.

As illustrated in Table III, the proposed converter and the converter in Fig. 9(a) have the minimum number of primary components. A small number of primary devices mean not only cheaper bill-of-material cost but also a simple and compact primary structure. As proved in Table IV, two flying capacitors in Fig. 9(b) sustain higher current stress. Hence, a high capacitance is required to minimize the voltage ripple applied on these capacitors. High VA rating and capacitance corresponds to a large volume of these capacitors.
As shown in Table IV, the current stress of the primary switches in Fig. (b) is extremely uneven. The current stress of S3 and S2 is approximately three times greater than that of S1 and S4. The uneven current stress distribution may cause several problems, i.e., selection of appropriate switches, current sharing among parallel connected components, and complexity of drive circuit and designing of heat sink. These problems are the drawback of the converter in Fig. (b). During normal operation, the current stress of Dcl1 and Dcl2 in the proposed converter is zero; according to Table IV, the current stress of Dcl1 and Dcl2 in the proposed converter is also smaller during a soft start operation. Thus, the required semiconductor area of Dcl1 and Dcl2 and corresponding heat sink of the proposed converter is smallest among the three converters. Furthermore, less current stress of Dcl1 and Dcl2 means a small reverse recovery problem; thus, the main switches in the proposed converter can be kept safely in the safe operating area even during fast dynamic instant. As proved in [1] and [21], the primary current flows through clamping diodes during freewheeling stages. Thus, the clamping diodes and the main switches in Fig. 9 are strongly recommended to be integrated into a power module by the producer to ensure safe operation. Although the producers of power electronics devices have provided some type-integrated diode-clamped TL power modules, the voltage and current ratings, selected range, cost, and the performance of these modules is still more unsatisfactory than that of widely used two-level HB power modules. Therefore, the proposed converter allows users to achieve high input DC–DC power conversion by easily available, cheap, and good-performance two-level power modules without sacrificing safety.

The VA rating of power transformers in Fig. 9 (a) is smaller in variable input voltage and constant output voltage applications. When the input voltage range is 2:1, the total VA rating is approximately 0.67 times that of the other two converters [19]. However, in constant input voltage and variable output voltage applications, the three circuits have the same VA rating for the transformers. The output inductance of the converter in Fig. 9 (a) is approximately three times that of other converters because the secondary rectified voltage is a two-level waveform. Furthermore, the volume of the input filter of the converter in Fig. 9 (a) is also the largest among the three converters. Thus, the overall magnetic component volume of the proposed converter and the converter in Fig. 9 (b) is smaller than that of Fig. 9 (a). As shown in Table III, the proposed converter has the maximum secondary power device number. The required semiconductor area of the secondary power devices in the proposed converter is also the highest.

The power loss comparison in Table V is estimated based on the parameters used in the prototype. The input voltage is 600V, and the output is 300V/40A. As shown in Table V, the proposed converter has the smallest primary power loss caused by the minimum switching loss and no freewheeling circulating conduction loss. For the secondary side, the power
loss in the proposed converter is slightly higher because of 
the added secondary switches. However, the added switching 
loss is smaller because of the ZCS operation, and the added 
conduction loss is also smaller because of the smaller 
conduction resistance of the secondary switches. Therefore, 
the proposed converter will have higher efficiency among the 
three converters, particularly under light loads, high 
frequency, or high input operation.

IV. EXPERIMENTAL RESULTS

The performance of the proposed converter is verified by a 
15 kW (300 V/50 A) prototype and the input voltage is varied 
from 600–800 V. The main parameters of the prototype are as 
follows: primary switches (IGBT), 75A/600 V; secondary 
switches (MOSFET), 61A/250V*4; rectifier diodes, 
200A/1200V; \( k_{T1}=4.03 \); \( k_{T2}=1.33 \); \( L_o=0.1 \) mH; \( C_o=1000 \) \( \mu \)F; and switching frequency, 20 kHz. To ensure safe ZVS for the 
primary switches, \( I_m \) is set as 60% of the maximum 
equivalent output current in the primary side \( I_{o,max}/k_{T2} \).
In the efficiency test, the converters in Fig. 9 are also tested for 
comparison, and these converters are designed on the same 
baseline.

As shown in Figs. 10(a) and 10(b), the off-state voltage of 
the primary switches in the proposed converter is even, and 
the midpoint voltage of the input capacitors is stable and 
equals \( V_{in}/2 \). As proven in Fig. 10(c), the voltage applied to 
the primary coil is \( V_{in}/2 \), and \( i_{Lk} \) is not a constant value 
because \( i_m \) is enlarged to help the ZVS of the primary 
switches. The added primary RMS current is smaller because 
\( i_m \) is not in phase with the load current. Thus, the added 
conduction loss is also smaller. The duty ratio of \( T_p \) is 100% 
and uncontrolled during the whole operation stages, which 
means no primary freewheeling circulating conduction loss 
ocurred. The secondary rectified voltage and \( i_{Lk} \), are provided 
in Fig. 10(d). As proven in Fig. 10(d), the secondary rectified 
voltage is a TL waveform, which can significantly reduce the 
volume of the output filter. The output voltage is adjusted by 
changing the time of \( V_{in}/2k_{T2} \) in Fig. 10(d). The ZVS 
characteristics of the primary switches in the proposed 
converter are tested with 10% load current. The waveforms of 
the gate signals and the collector–emitter voltages of switches 
\( S_1 \) and \( S_4 \) are depicted in Figs. 10(e) and 10(f). In Fig. 10(e), 
the gate–emitter voltage of \( S_1 \) is much lower than the 
gate–emitter threshold voltage when the collector–emitter 
voltage of \( S_1 \) decreases to zero; thus, \( S_1 \) can obtain ZVS. As 
shown in Fig. 10(f), \( S_4 \) can also obtain ZVS in a wide load
range. The waveforms of the drain–source voltage and current of Sse1 are shown in Fig. 10(g). As shown in the figure, Sse1 can obtain ZCS. The primary voltage and current waveform during soft start operation is provided in Fig. 10(h).

Fig. 11(a) shows the efficiency comparison under different load currents with 600 V input voltage. The proposed converter has higher efficiency because all the switches can obtain ZVS in a wide load range. The efficiency comparison under different input voltages with 40 A output is provided in Fig. 11(b), and the efficiency curves of all the converters decrease the increase in input voltage. The decreasing slope of the proposed converter is smaller than that of others because the magnetizing inductance can provide more resonant energy. Thus, the proposed converter is more suitable for high-input applications.

V. CONCLUSION

A new four-primary-switch diode-clamped soft switching TLDC with full ZVS load range and TL secondary voltage waveform has been proposed. The operation principle and characteristics of the presented converter are discussed, and the experimental results are consistent with theoretical predictions. The improvements of the proposed converter include a simple and compact primary structure, TL secondary rectified voltage waveform, wide load range ZVS for all primary switches, and full output regulated range with soft switching operation. The proposed converter also has some disadvantages. The VA rating of the transformer is slightly larger than that of conventional TLDCs in variable input and constant output mode. The conduction loss of the primary coil is slightly higher because an air gap is inserted into the magnetic cores of the transformer. Finally, the secondary circuit is slightly complex.

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