Design and Implementation of a SDR-based Digital Filter for CDMA Systems

Bong-Guk Yu, Young-Jo Bang, Dae-Ho Kim, Kyu-Tae Lee, Sung Woong Ra

Abstract—In this study, Software Defined Radio (SDR) technology-based digital filterbank architecture applicable to a multiple-channel processing system such as a wireless mobile communication system using Code Division Multiple Access (CDMA) technology is proposed. The technique includes a micro-processor to redesign Finite Impulse Response (FIR) filter coefficients according to specific system information and to download the filter coefficients to one digital Band Pass Filter (BPF) to reconfigure another system. The feasibility of the algorithm is verified by computer simulation and by implementing a multiple-channel signal generator that is reconfigurable to other system profiles, including those of a Wideband Code Division Multiple Access (WCDMA) system and a CDMA system.

Index Terms—Software Defined Radio (SDR), Filter, FIR, WCDMA, CDMA.

1 INTRODUCTION

MULTIPLE-channel systems such as second-generation digital mobile systems, Interim Standard (IS)-95 Code Division Multiple Access (CDMA) systems with a frequency bandwidth of 1.25 MHz for each Frequency Assignment (FA), and third-generation Wideband Code Division Multiple Access (WCDMA) systems with a 5 MHz bandwidth for one FA necessarily require a filtering operation to process each channel using a filter bank [1]-[2]. As a mobile communication service provider that deploys a mobile communication network with a CDMA system generally uses a multiple channels, equipment such as a CDMA signal generator or a relay using the CDMA technology must generate or relay multiple FA signals. Such a multiple-channel system necessarily requires a filtering operation using a filter so as to pass only a desired band of signals and not pass a non-desired band of signals. Usually, analog Surface Acoustic Wave (SAW) filters are normally used in IF (Intermediate Frequency) bands for a cellular handset and a relay station for cellular mobile communication [3].

In multiple-channel processing systems, the number of Band Pass Filters (BPF) used to process a channel signal is equal to the number of channels processed by the BPF [4]. Therefore, a conventional multiple-channel processing system is limited as both the size and cost increase as the number of processed channels increases. In addition, each multiple-channel system has its own system bandwidth. Upcoming 4G mobile systems based on Orthogonal Frequency Division Multiplexing (OFDM) technology have a range of system bandwidth profiles [5]-[7]. Thus, a type of software radio architecture that can flexibly adapt to a range of system profiles is required for multiple-channel filtering processing [8]-[9].

Software Defined Radio (SDR) technology is a promising feature for the next generation

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of mobile communications and the associated measurement system. It makes it possible to reconfigure required system profiles through software changes on an identical hardware platform. As it adopts software technology and various DSP (Digital Signal Processing) technologies such as digital filtering onto the IF and RF areas due to recent increase in the Analog-to-Digital Conversion (ADC) sampling speed, it is able to provide a high-performance and cost-effective solution in different systems [10].

The purpose of the present study is to provide a SDR-technology-based digital filter bank architecture that incorporates the advantages of changing the filter coefficients of one digital BPF and enabling the selective processing of each channel, thereby providing an efficient multiple-channel processing system. The feasibility of the algorithm was verified by implementing a multiple-channel signal generator that is reconfigurable to other system profiles, including those for a WCDMA system and a CDMA system. This paper is organized as follows. In Section 2, the novel digital filterbank architecture using one digital filter is presented. In Section 3, implementation of the multiple-channel signal generator is discussed, and its experimental results are presented to verify the suggested filtering algorithm. Finally, conclusions are presented in Section 4.

2 Design of Reconfigurable Filterbank Architecture

In this section, the suggested SDR-based reconfigurable digital filterbank architecture is introduced. A general block diagram of digital filter bank for a multiple-channel processing system is shown in Fig. 1. The typical digital filterbank includes M number of BPFs, and the output signal $y(k)$ is the sum of the signal output by filtering an input signal $x(k)$ according to the switch selection through the first to the M-th BPFs.

The conventional structure of a general Finite Impulse Response (FIR) BPF of the digital filterbank shown in Fig. 1 is presented in Fig. 2. As shown in Fig. 2, when the digital FIR BPF has N-numbered filter taps, the filter includes N-1 delay elements. Here, filter coefficients

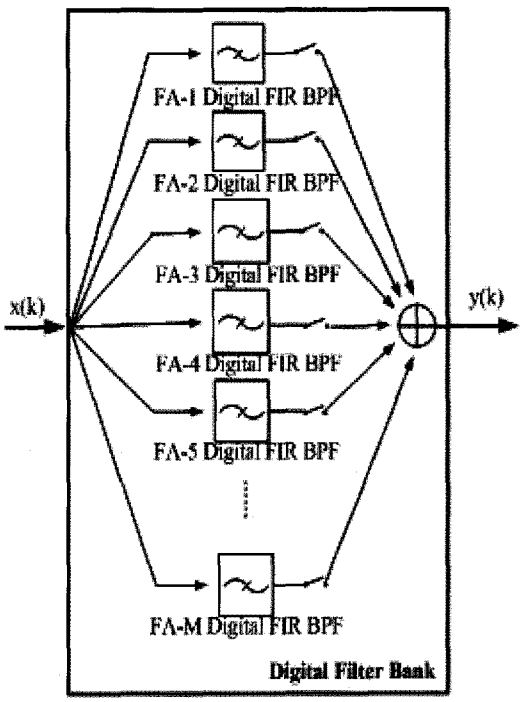


Fig. 1. Typical digital filterbank

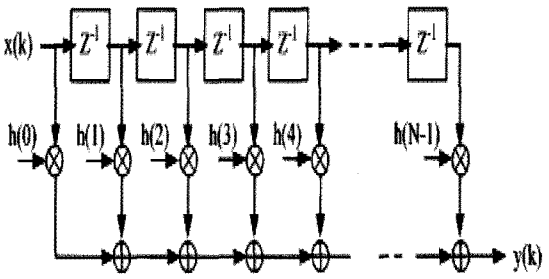


Fig. 2. Conventional digital FIR filter structure

$h(n)$ respectively multiplied to signals passing through the first to $(N-1)$-th delay elements are denoted as $h(0)$, $h(1)$, $h(2)$, ..., $h(N-1)$.

In Fig. 1, if the digital filterbank of a general multiple-channel processing system includes M numbered BPFs, the output signal $y(k)$ is the sum of the signal output after filtering an input signal $x(k)$ according to the switch selection for each channel, as in the following equation:

$$\begin{aligned} y(k) &= w_1 y_1(k) + w_2 y_2(k) + \ldots + w_M y_M(k) \\ &= w_1 \sum_{n=0}^{N-1} h_1(n)x(k-n) \\ &+ w_2 \sum_{n=0}^{N-1} h_2(n)x(k-n) + \ldots \\ &+ w_M \sum_{n=0}^{N-1} h_M(n)x(k-n) \\ & w_m = 0, \ if \ \ FA = "OFF" \\ & w_m = 1, \ if \ \ FA = "ON" \end{aligned} \tag{1}$$

Here, N is the number of filter coefficients and w_m is defined as a variable that is either 0 or 1 according to the ON/OFF state of the channel as input information of individual system profiles.

The channel output signal of the m-th BPF represented by $y_m(k)$ can be achieved by the convolution of $x(k)$ with the m-th BPF which has the filter coefficient of $h_m(n)$. As shown in (1), in typical multiple-channel processing systems, the number of BPFs for processing multiple-channel signals is equal to the number of channels to be processed by the BPF. Therefore, the required number of BPFs increases as the number of processed channels increases. As a result, factors such as the implementation complexity, size and cost for processing a channel also increase.

This paper proposes simple and efficient digital filterbank architecture to replace multiple BPFs with one BPF using SDR technology. It involves the use of a micro-processor to calculate the filter coefficient of the BPF according to the input information such as the system profiles and the channel ON/OFF status information. The output signal $y(k)$ in (1) can be expressed as the following alternative form:

$$\begin{aligned} y(k) &= \sum_{n=0}^{N-1} \{w_1 h_1(n) + w_2 h_2(n) + \ldots \\ &+ w_M h_M(n)\} x(k-n) \\ &= \sum_{n=0}^{N-1} h_{all}(n)x(k-n) \end{aligned} \tag{2}$$

Here, $h_{all}(n)$, which is the impulse response of the overall digital filterbank, is the total sum of the filter coefficients for each channel, $h_1(n)$, $h_2(n)$, $h_3(n)$, ..., $h_M(n)$. In addition, the final filter coefficients $h_{all}(n)$ may be expressed with the $h_M(n)$ and the ON or OFF state information of each channel when all digital FIR BPFs have N filter taps.

$$\begin{aligned} h_{all}(n) &= \sum_{m=1}^{M} w_m h_m(n), n = 0, 1, 2, \ldots N-1 \\ & w_m = 0, \ if \ \ FA = "OFF" \\ & w_m = 1, \ if \ \ FA = "ON" \end{aligned} \tag{3}$$

Where

$$\begin{aligned} h_m(n) &= h_B(n) \cdot f_m(n) \\ &= h_B(n) \cdot exp(j2\pi f_m n/f_s) \\ & m = 1, 2, \ldots M \end{aligned} \tag{4}$$

Here, $h_B(n)$ is a Low Pass Filter (LPF) coefficient, $f_m(n)$ is the center frequency of the m-th channel, and f_s is the sampling frequency.

Using the suggested filtering method based on digital low-IF technology, M BPFs with the filter coefficients $h_m(n)$ can be replaced by one BPF with the final filter coefficients $h_{all}(n)$. Fig. 3 is a flowchart showing the generation of the filter coefficients, $h_{all}(n)$ in a micro-processor. Here, M is the total number of channels and N is the total number of filter taps.

The processor determines whether the channel is in an ON state or an OFF state corresponding to the channel information entered through the user interface. If the channel is determined as in an ON state, the processor calculates the filter coefficients using the equation below and stores these values in the memory.

$$\begin{aligned} & f_{fa} = j * f_{ch} + f_1; \\ & I : h_{all}(i) += h_B(i) * \sin(2 * \pi * f_{fa}/f_s); \\ & Q : h_{all}(i) += h_B(i) * \cos(2 * \pi * f_{fa}/f_s); \end{aligned} \tag{5}$$

Here, f_fa, f_{ch}, f_1, and f_s represent the center frequency of each FA, the FA spacing, the center frequency of the first FA, and the sampling

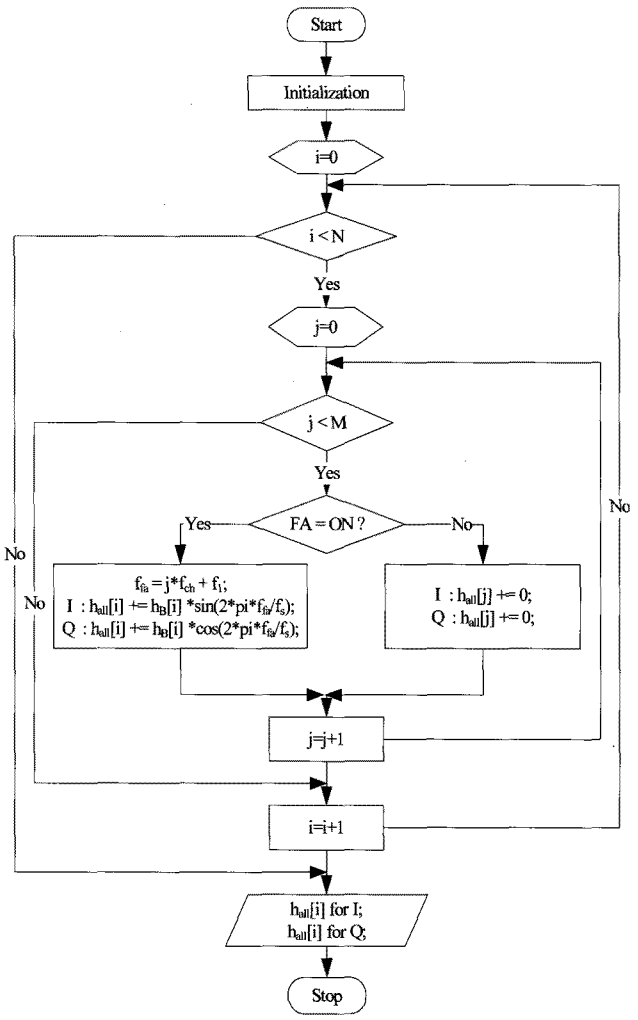


Fig. 3. Flowchart of the proportional filter coefficients design algorithm

frequency, respectively. In 5, $h_B(n)$ is given as a LPF coefficient of the system and $h_{all}(i)$ is a value obtained by accumulating a given calculated value to a $h_{all}(i)$ value as the calculated sum of the previous channel. Equation (5) expresses (4) as in-phase and quad-phase filter coefficients, which are orthogonal modulation values.

The micro-processor, which stores the initialization values shown in Table 1 for each system profile, the total number of channels of the system, the number of taps, the low-pass filter coefficients, the sampling frequency, the spacing between the channels, and the center frequency of the first channel, generates a filter coefficient using the information according to

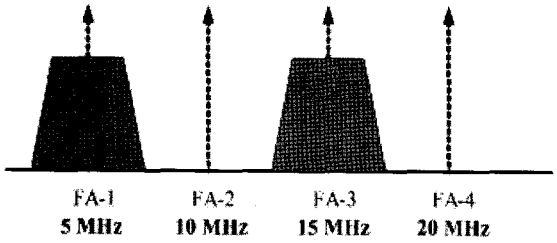
TABLE 1
Initialization Variables

Variables	Descriptions
M	total number of FAs of a multiple-channel system
N	number of taps
$h_B(n)$	low-pass filter coefficients
f_s	sampling frequency [MHz]
f_{ch}	FA spacing [MHz]
f_1	center frequency of 1^st FA [MHz]

the application of the channel selection signal. This information may be received from a channel selection input unit or may be programmed by the micro-processor in advance.

For example, if the total channel numbers of the multiple-channel system M is 4, if the channel spacing is given as 5 MHz, and if the center frequency of the first channel is given as 5 MHz, the center frequencies from the first channel to the fourth channel are obtained as 5, 10, 15, and 20 MHz, respectively. The controller receives the four-bit signal "1010" as the selection information from the channel selection input and stores the ON/OFF information of each channel, for example where the first channel = "ON", the second channel = "OFF", the third channel = "ON", and the fourth channel = "OFF". After the controller stores each channel as ON or OFF, the controller calculates the final N low-IF band filter coefficients by multiplying the center frequencies, $f_j = \sin(2*\pi*f_{fa}*t)$ for the in-phase signal and $f_j = \cos(2*\pi*f_{fa}*t)$ for the quad-phase signal of each ON state channel to the predetermined LPF coefficient of $h_B(n)$. It then sums the multiplied values. The controller generates a filter coefficient using the center frequency and the ON/OFF information of each channel such that the output spectrum shown in Fig. 4 may be output.

The multiple-channel filterbank system according to the suggested SDR-based digital filtering technique is shown in Fig. 5. The controller in Fig. 5 receives system profiles and channel selection information and calculates the filter coefficients $h_{all}(n)$ of the BPF so that it may simultaneously and selectively generate at least one channel by one BPF.



FA-1 = 5 MHz
FA-2 = FA-1 + f_{ch} = 10 MHz
FA-3 = FA-2 + f_{ch} = 15 MHz
FA-4 = FA-3 + f_{ch} = 20 MHz

Fig. 4. Signal generation example(when M=4)

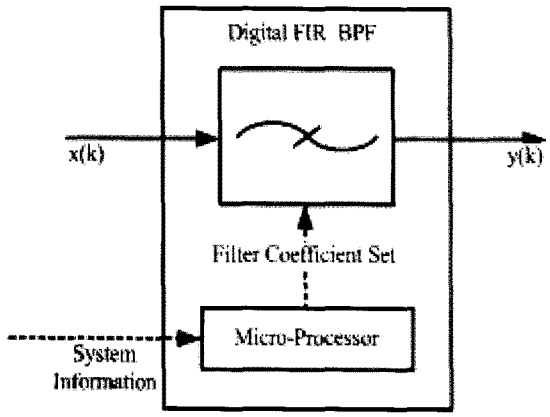


Fig. 5. Suggested digital filerbank Structure

3 Implementation and Test Results of a Multiple-Channel Signal Generator

In this section, simulation results of the proposed algorithm and the implemented multiple-channel signal generator to verify the feasibility of the proposed algorithm is presented for the specific system profiles such as WCDMA and CDMA system. Fig. 6 shows a block diagram of the implemented multiple-channel signal generator, and includes a micro-processor, an input signal generator, a digital BPF, a FIR controller, and a digital-to-analog converter (DAC).

The user interface is used to enter system information such as the system profiles and channel information of the state ON or OFF

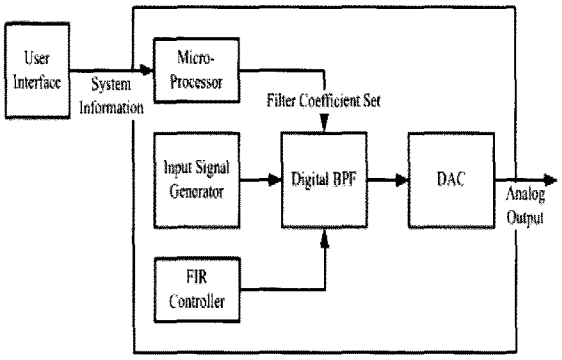


Fig. 6. The architecture of the implemented multiple-channel signal generator

TABLE 2
Initialization Variables of the Implemented System Profiles

Variables	System Profiles	
	WCDMA	CDMA
M	4	14
N	240	960
$h_B(n)$	-	-
f_s	50	50
f_{ch}	5	1.25
f_1	5	3.75

of the respective channels. This can include equipment such as a computer, a user terminal, and a keypad. The signal transmission between the user interface and the micro-processor located in the multiple-channel generator can be realized by a universal input/output serial interface. The micro-processor, which stores the initialization values shown in Table 2 for each system profile, generates filter coefficients $h_{all}(n)$ according to the algorithm shown in Fig. 3. The micro-processor then reconfigures the digital BPF by downloading the filter coefficients.

The input signal generator generates an input signal that is applied to the digital BPF. The generated signal may be a random signal or a PN sequence signal, as the implemented multiple-channel generator is used as a signal generator with the suggested algorithm. If the suggested filtering algorithm is used with IF signal filtering for a CDMA relay system, the input may become an uplink CDMA signal that is transmitted to the base station.

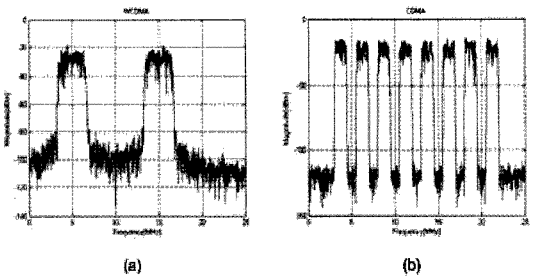


Fig. 7. Simulated output spectrum of a WCDMA system(a) and a CDMA system(b)

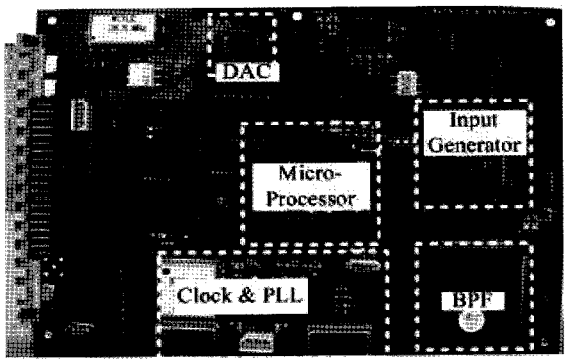


Fig. 8. Appearance of the multiple-channel signal generator hardware

The BPF filters the input signal applied from the input signal generator using the changed filter coefficient and outputs the filtered signal. The digital BPF is reconfigured to other system profiles through downloading with a filter coefficient set in real time. The filter coefficient of the digital BPF is changed according to the application of the filter coefficient generated by the controller. The BPF can be a Field Programmable Gate Array (FPGA) or a digital signal processor chip. Next, the FIR controller provides a control signal and an operation clock signal for the digital filtering of the BPF in real-time, and controls an internal register configuration that drives the DAC. The DAC converts the digital signal that is output after filtering by the BPF into an analog signal for measurement. Additionally, the DAC output signal can be up-converted to a higher RF band signal.

The suggested algorithm was simulated with MATLAB to verify the feasibility according to the flow chart shown in Fig. 3. The initialization variables adopted for the simulation have parameters that are identical to those on Table 2. The simulation results are shown in Fig. 7 for a WCDMA system and a CDMA system, respectively. The figure shows that the proposed algorithm using one BPF with the previously designed LPF filter coefficients successfully generates the multiple-channel signals that are centered on each different channel frequency.

The implemented hardware board of the multiple-channel signal generator is shown in Fig. 8. It includes a commercial-off-the-shelf (COTS) digital FIR filter chip, a micro-processor, a clock supply module, Complex Programmable Logic Devices (CPLD), and a DAC. The adopted FIR filter chip has a maximum operating speed of 83 MHz and filter coefficients with a resolution of 12 bits. A Z-80 series micro-processor is in charge of the operational control of the overall system, the user interface, and the filter coefficient calculation according to the intended system profiles. The micro-processor has a maximum clock speed of 30 MHz, a 20-bit address bus and an 8-bit data bus. A commercial DAC chip, the AD9772 by Analog Devices was used; converts a filtered digital signal to an analog signal [11]. The chip, which has 14-bit resolution, can operate at a maximum conversion rate of 160 Msps and shows 74 dBc of Spurious Free Dynamic Range (SFDR) when the input analog bandwidth is 25 MHz. The DAC chip operates at an on board system clock speed of 50 MHz.

Fig. 9(a) shows the output signals of the implemented multiple-channel signal generator at a low IF spectrum. In the example shown in Fig. 9(b), the BPF is reconfigured according to the filter coefficients generated by the micro-processor according to the user interface applying the WCDMA system profile and channel selection information to activate the first and third channels. Fig. 9(b) illustrates the output signals of the generator when reconfigured to a CDMA system.

Normally, RF performance tests such as an Inter-Modulation (IM) performance test of RF devices, antennas, relay systems, and cables

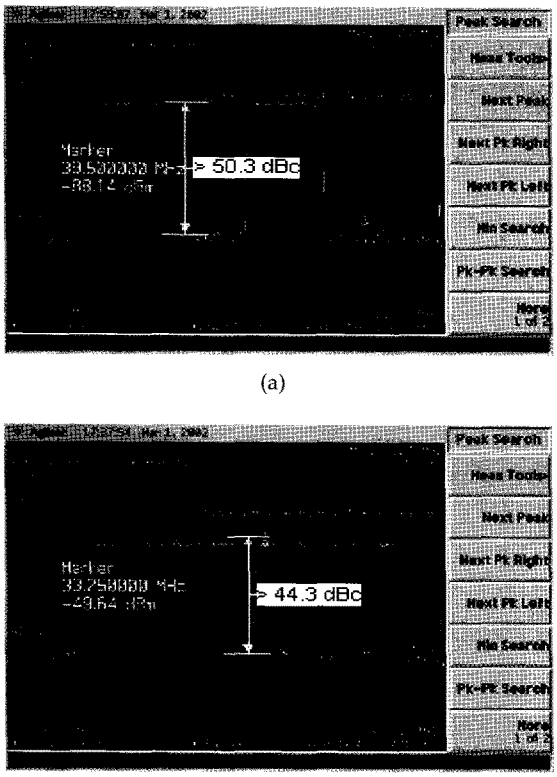


Fig. 9. Output of the generator when reconfigured to a WCDMA system (a) and to a CDMA system (b)

require at least two simultaneous signal generator outputs. However, these tests can be cost-effectively performed using a single set of equipment when adopting the proposed algorithm. Moreover, SDR technology enables the multiple-channel signal generator to be reconfigurable to other standard profiles that have been adopted in existing cellular, PCS, WCDMA or OFDM mobile communication systems through filter coefficients that can be downloaded onto identical hardware platforms.

4 CONCLUSIONS

In this paper, a novel digital filtering algorithm based on SDR technology that enables reconfiguration to other system profiles through software changes is proposed. The proposed algorithm uses one digital FIR filter to process multiple channels, enabling it to provide the simple and efficient filtering typically used in the relay system of a mobile communication system. Therefore, if the proposed algorithm is applied to a cellular relay system, the analog SAW filter and the RF switch in such a system can be replaced with one digital BPF using SDR technology regardless of the system profile.

Additionally, an implemented multiple-channel signal generator that can support WCDMA and CDMA profiles is presented. This verifies the feasibility of the proposed algorithm, as shown in computer simulation results. SDR technology enables the digital filterbank to be reconfigurable to other standard profiles, such as that of a multi-code CDMA system, through filter coefficients that can be downloaded onto identical hardware platforms. In the same way, any type of signal can be generated, including those used in upcoming fourth-generation mobile systems based on multi-channel OFDM technology.

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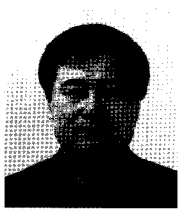

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